Flip Chip Assembly Process Development, Reliability Assessment and Process Characterization For Polymer Stud Grid Array-Chip Scale Package

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Abstract

The Polymer Stud Grid Array (PSGA) package is a new and unique type of area array chip scale package that shows significant advantages over conventional package configurations by virtue of its high potential for miniaturization and process cost saving potential.

This paper focuses on two key elements of PSGA technology which are: 1) developing a high throughput flip chip assembly process technology for PSGA-CSP configurations using existing Surface Mount Technology (SMT), and 2) qualifying the reliability performance of flip chip PSGA packages. The flip chip interconnection system evaluated is eutectic lead-tin solder. Various flip chip strategies are screened based on underfill materials and associated flip chip process technology. The underfill materials selected for evaluation are no flow reflowable, fast flow snap cure encapsulants, and high performance underfill systems. This work discusses issues related to developing a robust high throughput flip chip assembly process and presents preliminary reliability based on air-to-air thermal cycling (-55ºC to 125ºC) of the assembled PSGA Chip Scale Packages (CSPs).

Introduction

The Polymer Stud Grid Array (PSGA) is a result of an overall conceptual innovation in response to an industry demand for a low cost-chip scale package. The key advantages of the PSGA-CSP are its relatively short and unique fabrication technology. The utility of the PSGA package lies in its ability to route out fine pitch chips into a coarser pitch area array footprint on standard printed wiring boards (PWB) at a comparatively low cost. This CSP is deemed suitable for applications in the computer, automotive, consumer electronics and telecommunications industries by virtue of its small size, proven thermal performance, and good second level reliability [2].

Multiple design combinations of the PSGA package exist to make it suitable for its intended diverse applications. Typical applications include those in the IT-sector such as notepads (PDA, PCMCIA), telecommunications (cellular phones), and automation (intelligent connectors). Table 1 shows the different combinations that are available. The wire bonded PSGA-CSP version has recently entered commercial production.

Table 1 : Design Combinations of PSGA-CSP

Design Combinations of PSGA-CSP	
Wire bonded PSGA-CSP	Cavity up
	Cavity down
Flip chip PSGA-CSP	Over the edge (OTE)
	Microvia

Objective

The objective of this work is to develop a high-throughput flip chip assembly process, assess the reliability and characterize the assembly process for an OTE PSGA-CSP. The OTE flip chip PSGA-CSP utilized for this work is a plastic injection molded 9 mm by 9 mm square, full area array, 0.4 mm thick, and 0.8 mm stud pitch package. Each package has a trace metalization layer of copper, electroplated nickel and immersion gold. Typical molded substrates are in a four-up configuration with a supporting framework making a 26.4-mm by 26.4-mm quad package as shown in Figure 1. Each stud on the underside of the package is 400 μm in diameter and 500 μm in height. Each quad of the flip chip PSGA-CSP has two 72-stud substrates and two 80-stud substrates as shown in Figure 1.

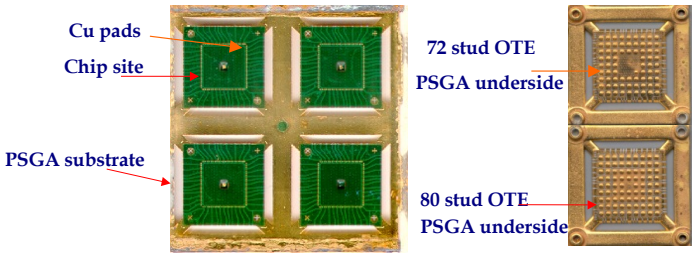


Figure 1 : OTE PSGA –CSP

The test chips utilized are daisy chained known good die supplied by Flip Chip Technologies. The chips have 88, 200-micron pitch, 120-micron diameter solder bumps in a perimeter array. The chips are 5mm by 5mm square and have a Silicon Nitride passivation layer.

Results of the preliminary flip chip assembly process development for the PSGA-CSP have been presented in [1] paper. The compatibility of the underfill-flux systems with the PSGA-CSP had been evaluated with partial success. Previous results have proven the reliability of the no flow underfill PSGA-CSP packages in liquid-to-liquid thermal shock (-55°C to +125°C) testing. The reliability of the no-flow underfill PSGA packages has since been evaluated in air-to-air thermal cycling (-55°C to 125°C) and the results are presented in this paper. In addition, the reliability of new material systems utilizing conventional and fast-flow snap cure underfills with compatible fluxes was also evaluated and shall be presented. The reliability of these new underfill-flux PSGA packages was also evaluated in air-to-air thermal cycle tests (-55°C to 125°C).

Assembly process development

The flip chip assembly process for this package was developed in three stages: placement process development, reflow profile development, and underfill dispense process development. Through every stage, existing knowledge of flip chip on board (FCOB) and Surface Mount Technologies (SMT) was leveraged towards developing a high throughput flip chip assembly process for the PSGA-CSP package.

Placement process development

Placement processes were developed for the PSGA-CSP for next-generation assembly packages using no-flow underfill as well as conventional assembly packages using dip and dispense fluxes. A fixture was designed and manufactured to enable accurate placement of the die. The details of the placement processes developed and the design and fabrication of the fixture are in [1]. Subsequent placement process development work has focussed on procuring a high throughput compatible fixture from a commercial vendor. This fixture, made of stainless steel, is pictured in Figure 2 and is capable of holding 7 PSGA-CSP quads.

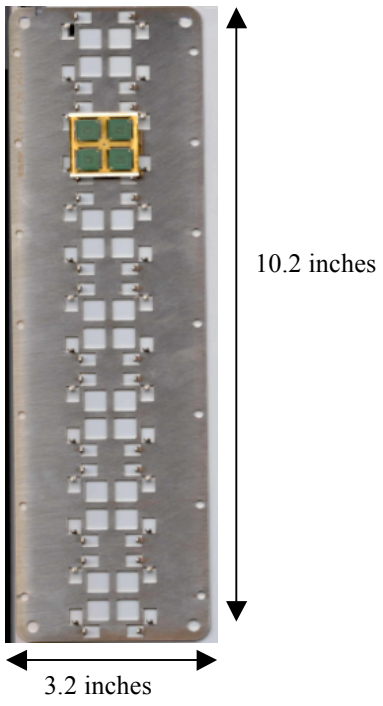


Figure 2: Commercial PSGA-CSP placement fixture

Reflow profile development

Reflow profiles were developed for a designated no-flow underfill A as well as dip flux A and dispense flux B previously. The reflow parameters for these profiles are presented in [1].

Additional fluxes were evaluated with the objective of choosing an underfill-flux system that maximizes overall package reliability. Hence reflow profiles were developed for dip fluxes A7 and B2. A BTU Paragon 7 zone reflow oven along with a WinKIC thermal profiling system was utilized for this work. The parameters of the reflow profiles developed are illustrated in Table 2. The actual profiles developed for fluxes A7 and B2 are pictured in Figures 3 and 4 respectively.

Table 2 : Reflow parameters for flux A7 and B2

Reflow parameters	Peak temp °C	Time between 110- 150C	Time between 150-183 C	Time above 183 C	Soak temp °C
Suggested profile for flux A7	210	NA	110 sec	50 sec	150
Actual flux A7 profile	216	NA	105 sec	56 sec	155
Suggested profile for flux B2	218	60-75 sec	120 sec	45-60 sec	160-180
Actual profile	219	71 sec	128 sec	65 sec	170

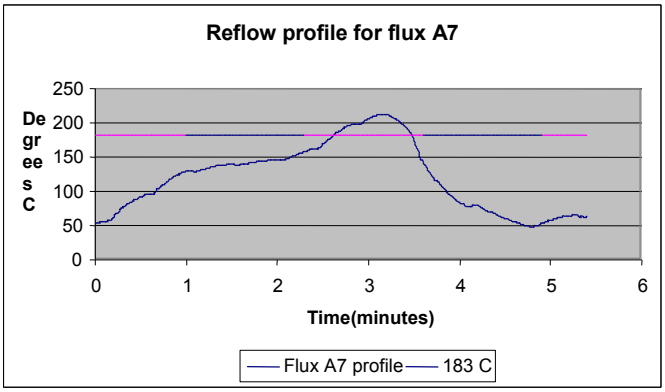


Figure 3 : Reflow profile for flux A7

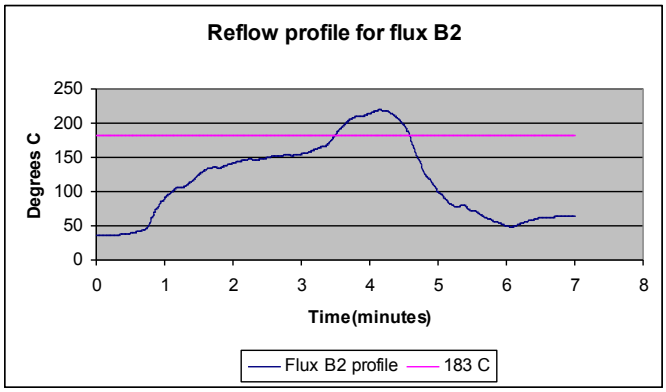


Figure 4: Reflow profile for flux B2

Packages assembled using fluxes A7 and B2 were subjected to die shear tests to inspect solder wetting and quality of interconnect formation. The resulting images proved that the solder balls satisfactorily wetted all the pads with the aid of the dip fluxes. Figure 5-A shows that the die assembled using flux A7 wetted all the pads on the package surface. This figure proves that all failures occurred at the die-solder bump interface resulting in the solder bumps being left behind on the package surface. Figure 5-B is a post shear close-up view of the top left-hand corner of the package surface. Figure 5-C is a close up of a single solder bump.

Figure 5-A

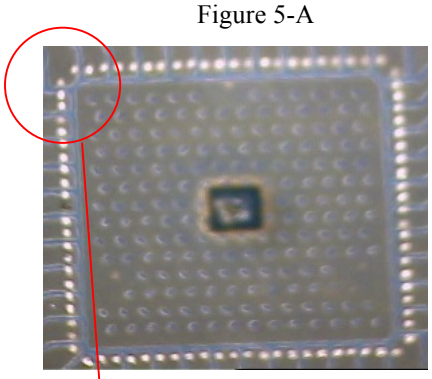


Figure 5-B

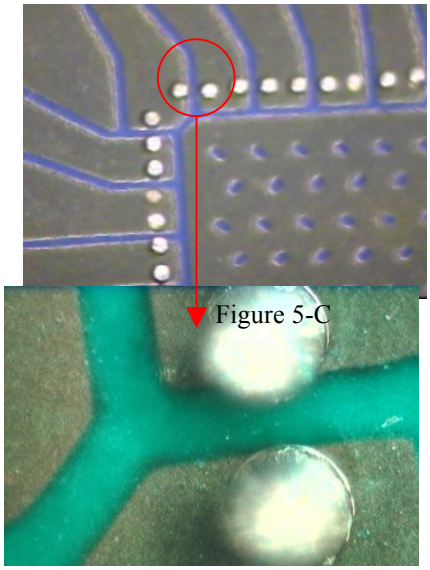


Figure 5-C

Figure 5: Post-shear images for PSGA-CSP module assembled using dip flux A7

Underfill dispense process development

Three types of underfill systems, no-flow, high performance, and a fast flow-snap cure underfill were selected for assessment with the PSGA-CSP packages. Table 4 below shows the underfills for which dispense processes were developed.

Table 3 : Underfills for which dispense processes have been developed

Underfill System type	No flow	High performance	Fast flow-snap cure
	Material A	Material B	Material D
		Material C	
		Material E	

A CAMALOT 1818 Liquid Dispensing System was utilized for developing a suitable dispense process. A 23 gauge needle was used for dispensing, and the package temperature was maintained at 90°C during the dispense process. The underfill was dispensed at a height of .025 in with a speed of .25 in/sec.

Details of the underfill dispense results for underfills A, B, C and D have already been presented in [1]. To summarize the previous dispense results, void free distribution of underfill was observed underneath the die for packages assembled by the next generation assembly process using no-flow underfill. For the high performance and fast flow-snap cure underfills, a one-pass underfill dispense method was adopted wherein underfill was applied along one side of the die and allowed to flow underneath it. This was followed by the dispensing of the fillets along the remaining three sides of the die. It was noticed that a void consistently occurred at the center of the package, Figure 6, for the underfills B, C and D. The location of this void coincided with that of a dimple on the underside of the PSGA-CSP package.

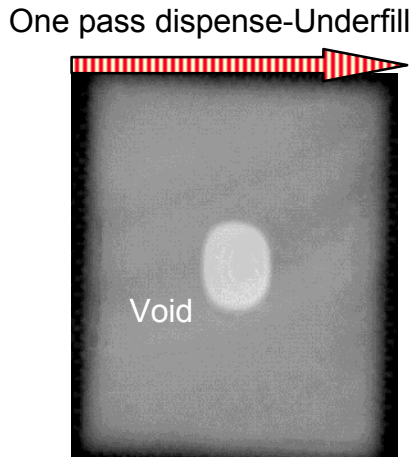


Figure 6 : Typical one pass dispense results for underfill D

Subsequent work focused on eliminating the void in the center. This was achieved by applying an L-pass dispense pattern where the underfill was dispensed along two adjacent sides of the die. This was followed by a wait time during which the underfill flowed across the underside of the die. The dispense of the fillets then followed along the remaining two sides. The success of this dispense pattern is evident from Figure 7 which shows a typical underfill distribution for high performance material E. Similar results have been obtained for fast flow-snap cure underfill D.

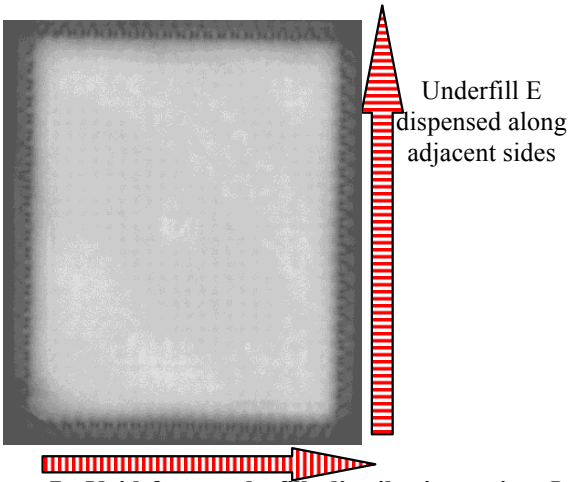


Figure 7: Void-free underfill distribution using L-pass dispense method

Assembly process development-Phase II

Previous process development work evaluated the reliability of one no-flow underfill A, two high performance underfills, B and C, with dip and dispense fluxes A and B and one fast flow-snap cure underfill D with the above two fluxes. Preliminary liquid-to-liquid thermal shock (-55^{o}C to +125^{o}C), JESD22-A106-A, reliability results for underfills A, B, C and D are summarized in [1]. Of the combinations evaluated the PSGA-CSP packages with no-flow underfill A fulfilled the pass-criteria.

The pass criteria for the underfill-flux combinations was that all underfill packages must pass 1000 cycles. An electrical failure was defined as a greater than 10% change in the measured package resistance. The resistance was measured using a two-point probe and a Keithley 9000 multimeter.

Based on the reliability performance of underfill A, this underfill was chosen for assembly. The first failure in the initial batch of these underfill packages when subjected to liquid-liquid thermal shock (LLTS) occurred after 1000 cycles. The air-to-air thermal cycle test, which will be used to qualify the reliability of these packages, is less harsh than the LLTS test. Hence, it is expected that the reliability performance of these underfill-PSGA-CSP packages will improve in air-to-air thermal cycling.

Fast flow-snap cure underfill D was selected for further evaluation with different flux combinations. A new high performance underfill E with compatible dip fluxes A7 and B2 was chosen for evaluation. Underfill D was also evaluated with the newly selected fluxes. Two different cure processes were applied to underfill systems D and E to determine the impact of each cure process on the reliability of the package. The first cure method, called B-staging, applied was to maintain the underfill at the gel temperature for the suggested length of gel time and then to cure it at its cure temperature for twice the recommended cure time. The second cure method was to straight cure the underfill for the manufacturer recommended length of cure time. Table 4 illustrates the underfill-flux-cure technique combinations evaluated below.

Table 4: Underfill-flux-cure technique combinations tested

Straight cure technique			
Fast-flow underfill D		High performance underfill E	
Flux A7	Flux B2	Flux A7	Flux B2
B-staged cure technique			
Fast-flow underfill D		High performance underfill E	
Flux A7	Flux B2	Flux A7	Flux B2

The sample size was restricted to 2 packages per treatment combination to conserve PSGA-CSP packages for future processing needs. The LLTS reliability results for underfills D and E using fluxes A7 and B2 and the two cure processes are summarized in Tables 5 and 6 respectively.

Table 5: Phase II reliability results for straight cured underfill-flux systems

Underfill-flux system		Cycles to first failure	# samples passed 1000 cycles
Fast-flow snap cure underfill D	Flux A7	1400	2/2
	Flux B2	900	1/2
High performance underfill E	Flux A7	1700	2/2
	Flux B2	1400	2/2

Table 6: Phase II reliability results for B-staged cured underfill-flux systems

Underfill-flux system		Cycles to first failure	# samples passed 1000 cycles
Fast-flow snap cure underfill D	Flux A7	1700	2/2
	Flux B2	1000	2/2
High performance underfill E	Flux A7	1700	2/2
	Flux B2	In test @1900	2/2

B-stage curing the samples was eliminated as a processing option as it would increase assembly time during high volume production of these packages. Flux B2 was eliminated on the premise that both underfill samples with this flux delaminated at 1000 cycles. Hence, flux A7 along with the two underfill systems D and E was chosen for the final assembly. Given that the failures occurred well after 1000 cycles for the chosen combinations, it was expected that the first failure for each of the underfill systems should be past 1000 cycles for a larger sample size. A complete listing of the material properties of the selected underfills is presented in Table 7.

Table 7: Material properties of underfills D and E

Material property		Fast-flow snap cure underfill D	High performance underfill E
CTE(ppm/C)	Alpha 1	28	45
	Alpha 2	104	143
Flexural Modulus(GPa)		7.6	5.6
Tg (C)		144	140
Viscosity @ 25C (cps)		10000	2300
Filler Content (%)		62	50
Gel time @ 121 C		6 minutes	13.5 minutes
Cure temp and time		160°C for 7 minutes	165°C for 30 minutes

Assembly process build of PSGA-CSP packages for reliability assessment

Next –generation flip chip assembly process using no-flow underfill A

100 packages with no-flow underfill A were assembled using the low cost-next generation assembly process, Figure 8, for further reliability assessment. 9 mg of no-flow underfill A was dispensed, using a Speedline Technologies CAMALOT 1818 underfill dispense machine, on each individual package of the PSGA-CSP quad prior to chip placement. The die was subsequently placed using the Siemens F5 placement system. A chip placement force of 4 N was used with a 100% acceleration factor. The samples were then subjected to the no-flow underfill reflow profile developed. 100 samples were produced using this method of assembly. The interconnect and die yield for this assembly are summarized in Table 8.

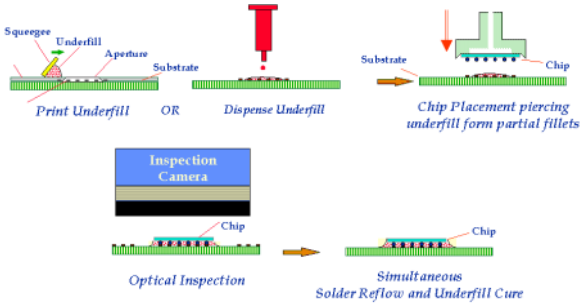


Figure 8: Low cost-next generation flip chip assembly process

Table 8: Interconnect and die yield for next-generation flip chip assembly process

#Bumps failed/ Total Bumps	% bump yield	#Die failed/ Total Die	% die yield	Other defects
23/8800	99.74	3/100	95%	2 solder bridges

Conventional flip-chip assembly using pre-selected underfill-flux systems

As mentioned earlier, flux A7 and underfills D and E were selected for this assembly process pictured in Figure 9. The die was dipped in 55 microns of dip flux A7 prior to chip placement. A dip time of 2 seconds was used. The chip was placed with a force of 3 N and an acceleration factor of 100%. After this, the sample was subjected to the reflow profile for flux A7 as outlined in Table 2. The die yield for this assembly is outlined in Table 9 below.

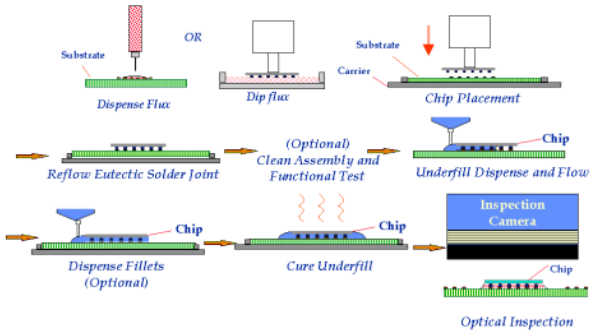


Figure 9: Conventional flip chip assembly process

Table 9: Die yield for conventional flip chip assembly process

Die assembled using profile for flux A7	#Die yield/ Total Die assembled	% die yield	Other defects
	142/156	91	None

Reliability results

Table 10 below summarizes the number of samples assembled and evaluated for each of the underfill flux combinations.

Samples of each underfill-flux combination were subjected to an air-air thermal cycle test.

Table 10: Number of samples of each underfill-flux combination evaluated

Underfill-flux combination evaluated for PSGA assembly	Total number of samples built for evaluation	Number of samples subjected to air-air thermal cycling tests (-55°C to +125°C)
No flow underfill A	100	27
Fast flow-snap cure underfill D with flux A7	69	30
High performance underfill E with flux A7	69	30

The air-air thermal cycles ranged from -55°C to +125°C. The dwell and cycle times at each temperature were 10 minutes each. The samples were tested for continuity every 100 cycles. X-ray and C-SAM images of the samples were recorded every 200 cycles.

Air-to-air thermal test results

Table 11 summarizes the results of the air-to-air thermal tests for each of the three underfill-flux systems.

Table 11: Results of air-to-air thermal cycling for evaluated underfill-flux-package systems

Underfill flux type	# of samples tested	Cycle to first failure	Cycle to last failure	Mean Life	Rate of failure/ 100 cycles after first failure
No-flow underfill A	27	2400	3900	3248	7.98
Fast flow-snap cure underfill D with flux A7	30	900	3000	1898	3.53
High performance underfill E with flux A7	30	1400	2300	1880	7.76

Figure 10 is a plot of the Weibull distribution of the air-to-air thermal cycling reliability results for the PSGA-CSP packages using no-flow underfill A.

Figure 10: Weibull distribution plot of air-air thermal cycle reliability results for PSGA-CSP packages using no-flow underfill A

Figure 11 is a plot of the Weibull distribution for the fast flow-snap cure underfill samples with flux A7 that were subjected to air-air cycling tests.

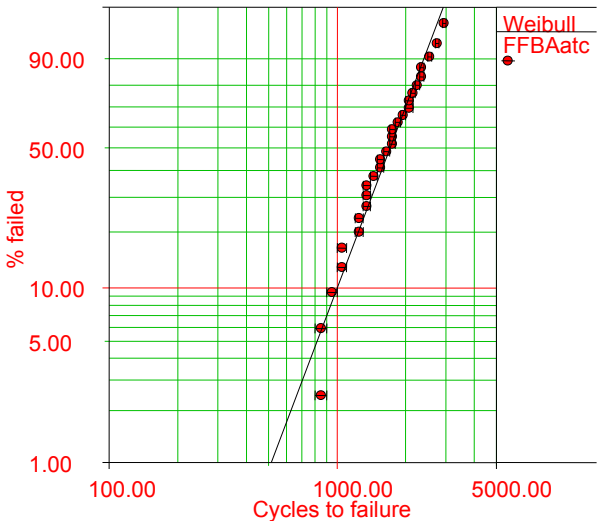


Figure 11: Weibull distribution plot of air-air thermal cycle reliability results for PSGA-CSP packages using fast-flow snap cure underfill D and flux A7

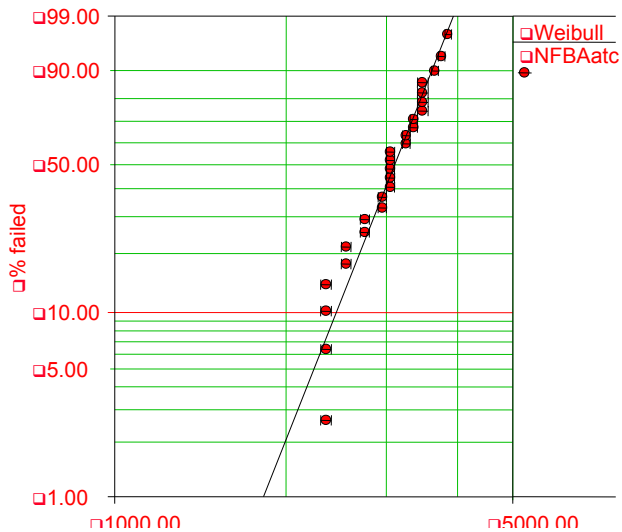


Figure 12 is a plot of the Weibull distribution for the high performance underfill E PSGA-CSP packages that were subjected to air-air cycling tests.

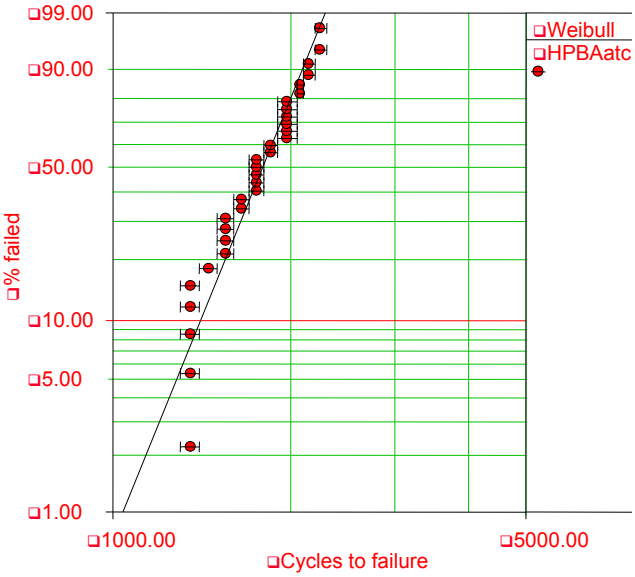


Figure 12: Weibull distribution plot of air-air thermal cycle reliability results for PSGA-CSP packages using high performance underfill D and flux A7

Process characterization

An assembly process characterization is necessary to gain an understanding of the critical factors affecting the outcome of a high-yield flip chip assembly process on the PSGA-CSP. Factors were identified and corresponding experiments were designed to characterize the placement, reflow and underfill dispense processes for both the conventional and next generation flip chip assembly processes.

Placement process characterization

The design of experiments, shown in Table 12, was generated in order to characterize the placement process for the conventional flip chip assembly process. The factors varied were placement force, dwell time, dip time and the height of the dip flux. One PSGA-CSP quad was assembled per treatment combination.

Trial	PI Force (Newton)	Dwell Time (Sec)	Dip Time (Sec)	Flux height (microns)
1	4	0.1	0	35
2	6	1	0	35
3	6	0.1	1	35
4	4	1	1	35
5	4	0.1	0	75
6	6	1	0	75
7	6	0.1	1	75
8	4	1	1	75
9	6	1	1	55
10	6	0.1	0	55
11	4	1	0	55
12	4	0.1	1	55
13	5	0.5	1	75
14	6	0.5	0.5	75
15	5	1	0.5	75
16	5	0.1	0	75
17	5	1	0	35
18	6	0.1	0.5	35
19	4	0.5	1	35
20	4	0.5	0	75
1	4	0.1	0	35
2	6	1	0	35
3	6	0.1	1	35
4	4	1	1	35

Table 12: DOE table for conventional assembly placement characterization

The electrical yield results for this characterization study are summarized in Table 13 below.

Table 13: Yield results for placement characterization

#Bumps yield/ Total Bumps	% bumps yield	#Die passed/ Total Die assembled	% die yield	Other defects
8712/8712	100	99/99	100	None

One PSGA-CSP assembly from each of the test quads assembled was subjected to cross-sectional analysis. Typical solder joints are shown in Figure 13 below.

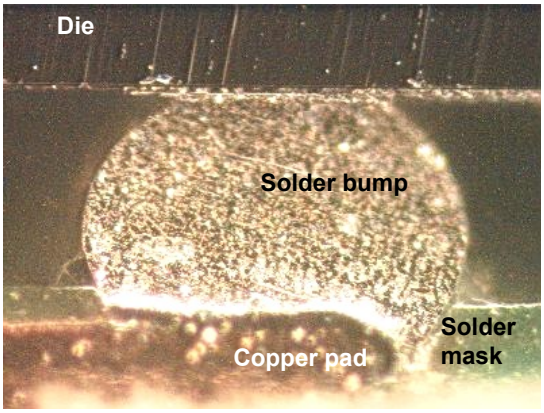
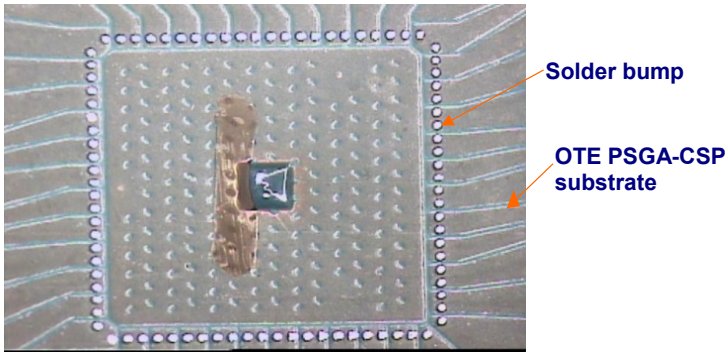


Figure 13: Solder joint in PSGA-CSP assembled using treatment combination 19 placement parameters

One PSGA-CSP assembly from each treatment combination was subjected to die shear tests. Typical post-shear PSGA-CSP substrates showing failures at the bump-die interface is shown in Figure 14 below.

Figure 14: Post-shear test PSGA-CSP substrate assembled using treatment combination 1 parameters



The electrical yield results, the cross-sectional analysis and the die shear tests suggest that the variations made in the placement parameters had no effect on the electrical yield of the package or the quality of the solder joints formed. Hence none of the placement parameters are critical relative to each other. Given this conclusion, the parameters may be changed to minimize the time required for placement.

A similar set of experiments to characterize the next generation chip placement process is proposed for future work.

Reflow Process Parameterization

A set of experiments was designed to parameterize the reflow process. Table 14 shows the parameters that were varied in order to parameterize the reflow. These parameters included soak temperature, ramp rate, soak time, time above 183 ^{o}C, and peak temperature. Reflow profiles that differed from the base profile by a single parameter setting were developed with the aid of a SlimKIC thermal profiling system. A profile was created for each of the parameters at the different settings. Other than the changed factor, the difference between the other parameters of the new profiles and those of the base profile was minimized. This is elucidated in Table 14.

A BTU Paragon, 7 zone reflow oven was used for the parameterization studies. The die were placed on the PSGA-CSP substrates using a Siemens F5 placement system. One quad was assembled for each reflow profile. Optimized placement parameters from the placement characterization process were applied.

Table 14: Reflow parameters varied

Parameter varied	**Parameter values (Reflow profile #)**		
Soak Temp(C)	130 (R1)	150 (R2)	170 (R3)
Soak Time(sec)	80 (R4)	110 (R5)	140 (R6)
T>183C	30 (R7)	50 (R8)	70 (R9)
Peak Temp(C)	200 (R10)	210 (R11)	220 (R12)

All reflow profiles except R1 and R9 resulted in 100% electrical yield. Hence the limits of the reflow window are established by the remaining successfully yielding profiles.

Underfill dispense optimization

As discussed earlier, the L-shaped underfill dispense pattern was selected for the conventional flip chip assembly process. A dispense process must result in a void free distribution of underfill and it is critical that the fillets formed on all four sides of the die are uniform in shape. Both these factors ensure that the stress is evenly distributed along the underside of the die. Additionally, the dispense process must be completed in the minimum time possible to facilitate maximum throughput of packages. The above three objectives, void free dispense, uniform fillet sizes and minimum dispense time was the focus of this optimization process for both the next generation assembly using no-flow underfill as well as the conventional assembly using epoxy underfills D and E.

Conclusions

A robust flip chip assembly process has been developed for the PSGA-CSP after evaluating different underfill-flux combinations. Both the next-generation assembly using a no-flow underfill and the conventional assembly using an underfill-flux combination were validated using liquid-to-liquid thermal shock tests. Subsequent PSGA-CSP package builds using the validated materials resulted in a high yielding assembly.

The reliability assessment of the assembled packages in air-to-air thermal cycle tests showed that the package-material combinations fulfilled the pass criteria of lasting 1000 cycles without any failures.

The placement process was characterized to establish a large placement process window. The reflow profile was parameterized to define the boundaries for a high throughput reflow process. The dispense of underfill for the conventional assembly process has been optimized to consistently result in a void free dispense with uniform fillets in minimum process time.

Future work

Subsequent work shall focus on characterizing the next generation placement process using no-flow underfill. A design of experiments has been prepared and shall be implemented. Alternate die and substrate cleaning techniques such as plasma cleaning shall be applied with the objective of increasing the reliability of the PSGA-CSP packages.

References

[1] Paydenkar C et al., "Chip Scale Polymer Stud Grid Array Packaging and Reliability Based on Low Cost Flip Chip Processing", Proceedings of the 50th Electronic Components and Technologies Conference, Las Vegas, USA, May 2000.

[2] Vandevelde B. et al., "Reliability Assessment for the Polymer Stud Grid Array Package", 37th IMAPS Nordic Conference, Helsingor, 2000.