EVALUATION, OPTIMIZATION, AND RELIABILITY OF NO-FLOW UNDERFILL PROCESS

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ABSTRACT

The advent of no-flow fluxing underfills for Flip Chip on Board application has required a new investigation of optimal processing for increased reliability. This research provides a systematic development of optimal process parameters for four commercially available fluxing underfills. The impact of the dispensing pattern on void formation is determined. DOE1 includes dispense pattern at 3 levels, and speed at 2 levels. Metrics include yield, material voiding, and fillet shape. Low temperature cure is used to isolate the effects of dispensing by avoiding any volatility of a standard reflow cure. The impact of the placement process is determined in a second experiment, DOE2, involving placement force, speed, and dwell time at 2 levels. Metrics include yield, underfill voiding, solder voiding, and electrical yield. The results of these experimental studies are used to select an optimal placement process for each material. Reflow parameters are investigated using a parametric approach. The following parameters are varied at 2 levels individually off a baseline profile: Peak Temperature, Time > 183 C, Peak Ramp Rate, Soak Time, and Soak Temperature. The results of these initial studies will be used to choose an optimal process for each material. Test boards were assembled according to the optimal process for each material, and AATC thermal cycling test was performed.

Key Words: Underfill, Flip Chip, Process Optimization

INTRODUCTION

Underfills are typically used in flip chip packaging to help mitigate the effects of the large Coefficient of Thermal Expansion (CTE) mismatch between the silicon chip and the laminate circuit board. The underfill acts to reduce the strain on the solder joints resulting in improved interconnect fatigue life [1].

The capillary flow underfill process involves fluxing, placing, and reflowing the flip chip first, and then dispensing the underfill along the sides of the chip. The underfill flows by capillary action to fill the area underneath the chip. Finally, a cure must be completed in an oven.

No-flow underfill processing utilizes fluxing underfills that are dispensed onto the substrate before placement. The die is then placed onto the dispensed underfill causing squeeze flow of the material during placement. The assembly is then reflowed and cured simultaneously in a standard reflow oven [2].

This paper presents a systematic optimization of the placement and reflow parameters for a no-flow process using four commercially available underfill materials.

EXPERIMENTAL METHODOLOGY

Four types of no-flow underfill materials were investigated: Underfill A, B, C, and D. One test vehicle was used for all assemblies. Prior to assembly the boards were baked out at 125 ºC for 3 hours. This bakeout time was determined from a previous bakeout experiment, and was sufficient to avoid outgassing of the boards. The boards were stored in a desiccant chamber after bakeout, for no more than 2 hours before assembly. Test vehicles for each experiment were assembled according to the procedures outlined later in the assembly process section. After assembly, the boards were analyzed using acoustic microscopy, x-ray, cross sectioning, and SEM.

Test Vehicle Description

The test vehicle consisted of an area array die mounted on a FR-4 substrate with six sites. The test die were supplied by Flip Chip Technologies and had daisy chain structures. The die were area array FA10-200x200 with 10 mil pitch. The trace metallization on the boards was copper, electroplated nickel, and immersion gold. The bond pads were hybrid having two sides mask defined and two sides pad defined. There are probe points on the substrates that allow continuity testing of the rows of interconnects. During continuity testing the row was considered failed if the loop

resistance deviated by more than 10% from the baseline resistance.

Assembly Process (DOE1)
Dispensing was done with an Asymtek millennium using a 22-gauge needle. Placement was done with a Siemens F5 Siplace for speed 1 (70 mm/s), and a K&S 6900 for speed 2 (5 mm/s). Both machines were calibrated for force and speed using a high-speed camera prior to running the experiment. The force used during DOE1 was 5N. The dwell time used was 0.10 seconds.

Boards were assembled according to the design matrix shown in Figure 1, for each underfill A, B, C, and D. Dispense patterns are shown in Figure 2. Each row of the matrix corresponds to one treatment in the DOE; four replicates were assembled for each treatment. The target dispense weight was 8 mg; actual dispense weight varied between 7.5 mg and 8.5 mg. The assemblies were low temperature cured at 130 ºC for 1 hour in an oven. The temperature was chosen to avoid reflow and any material volatility so that the effects of the factors included in the DOE could be studied in relative isolation from the reflow process.

Underfill A, B, C, D		
	Pattern	Speed (mm/s)
11	dot	70
12	dot	5
21	line	70
22	line	5
31	cross	70
32	cross	5

Figure 1. DOE1 Design Matrix

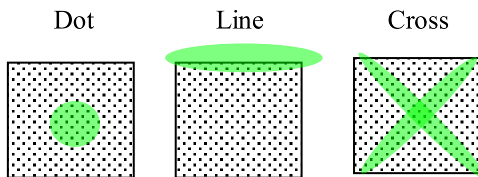

Figure 2. Underfill dispense patterns

After curing the boards were scanned using acoustic microscopy (CSAM) to identify voids. The captured images were analyzed with digital image analysis (DIA) software to obtain voiding reported in % area. After all the parts were scanned, they were then planar cross-sectioned and viewed optically under a microscope to determine if the CSAM image analysis was adequate for data analysis. For each underfill the CSAM images do not show many of the voids that are clearly present under microscope inspection after cross sectioning. Therefore, a manual count of the voids visible by optical microscope was used for statistical analysis. Response was reported in number of voids, rather than in % area. This technique can be expected to yield accurate data for comparison, because all the voids were roughly the same size, and most parts had many voids (>100) so that any differences in size can be expected to average out. JMP software was used to perform the statistical analysis.

Assembly Process (DOE2)
For each material, a full factorial DOE was used with three variables. Based on the results of the DOE1, dispense pattern was included with 2 levels: dot and line. Placement force was included at 2 levels: 1N and 5N. Dwell time was included at 2 levels: 0 and 0.1 seconds. All treatments were performed in replicates of 4. Interconnect yield percent was the primary metric; void area and fillet shape serve as a secondary metrics. Based on these experimental results, an optimal placement process for each material will be selected for further reflow profile experimentation.

Dispensing was done with a CAMALOT 3300 dispenser using a 22-gauge needle, due to the removal of the Asymtek millennium machine from the laboratory. Placement was done with a Siemens F5 Siplace. Reflow was accomplished using a BTU 7-zone reflow oven.

Boards were assembled according to the design matrix shown in table 2, for each underfill A, B, C, and D. Each row of the matrix corresponds to one treatment in the DOE; four replicates were assembled for each treatment. The target dispense weight was 8 mg; actual dispense weight varied between 7.5 mg and 8.5 mg. The assemblies were reflowed according to a baseline process; the reflow profiles were designed based on the material suppliers recommendations and were determined to yield 100% reliably when using both the dot or line pattern with force of 5N and .5 seconds dwell.

Underfill A, B, C, D			
	Pattern	Force (N)	Dwell (s)
111	**dot**	1	0
112	dot	1	0.1
121	**dot**	5	0
122	dot	5	0.1
211	line	1	0
212	line	1	0.1
221	line	5	0
222	line	5	0.1

Figure 3. DOE2 Design Matrix

After the boards were assembled according to the parameters in Figure 3, electrical continuity tests were performed to determine the percent interconnect yield. The boards were then scanned using acoustic microscopy (CSAM) to identify voids. The captured images were analyzed with digital image analysis (DIA) software to

obtain voiding reported in percent of total die area. The results were analyzed using JMP statistical software with percent voiding as the response.

Reflow Study

There are two distinct types of reflow profiles that were utilized in this experimental work; these types are described as either a step (Figure 4) or a ramp profile (Figure 5).

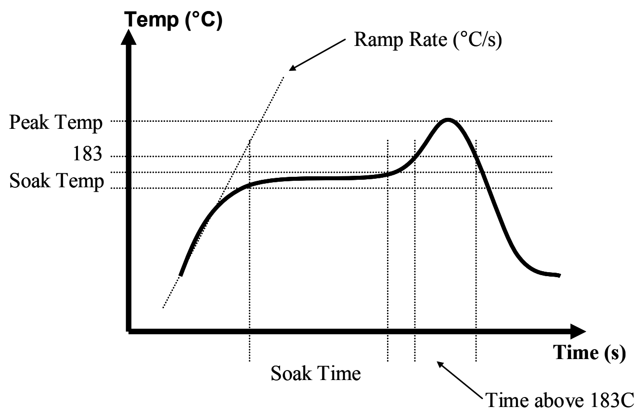

Figure 4. Step profile

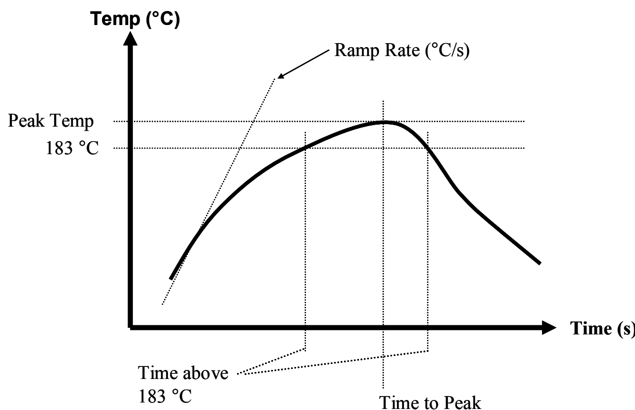

Figure 5. Ramp profile

There were two main goals of this experiment: to determine the optimal reflow profile for each material, and to define a reflow process window for each material. The experimental design was chosen to be a parametric study due to limitations on time and materials, as the requirements for a full factorial DOE would have been excessive.

A baseline reflow profile was developed for each material based on the manufacturers suggested profile. This profile was validated by placing 4 die and sending the assembly through reflow. The assemblies were then checked for continuity by resistance measurement. After a baseline profile was established, new profiles were generated by varying each of the profile parameters individually by an amount higher or lower than that of the baseline parameter value, while keeping all other parameters at or near their baseline value, see Figure 6.

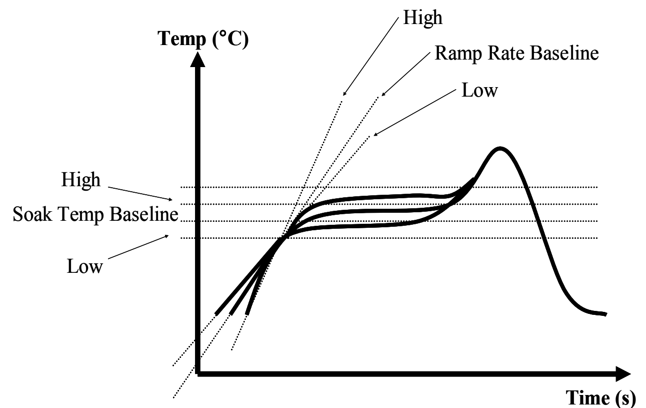

Figure 6. Reflow Profile Variation

For the step profile this hi/low variation produces 2 profiles for each reflow parameter shown in Figure 4, for a total of 10 distinct profiles for analysis. The ramp profile produces 8 profiles, 2 from each of the 4 parameters shown in Figure 5. Replicates of 4 die were assembled for each reflow profile, using the optimal dispense process from DOE1 and DOE2. For each reflow profile, die were assembled in replicates of 4.

RESULTS

DOE1

ANOVA shows very low p-values (<.001) for pattern, observed for all three underfills, indicating that dispense pattern is a significant factor affecting the number of voids occurring during placement. The Mean response for dot, line, and cross patterns was 141.3 voids, 3.7 voids, and 126 voids respectively. It seems likely that the capillary flow process associated with the line pattern is better at filling the solder mask openings without capturing voids during the process. The dot and cross patterns result in squeeze flow that has a tendency to capture voids during the rapid flow of the material. Line pattern was chosen to be included in DOE2 because it resulted in minimal voiding. The dot pattern was chosen instead of the cross pattern because the mean response was similar and the dot pattern is faster for ultimate use in a production process.

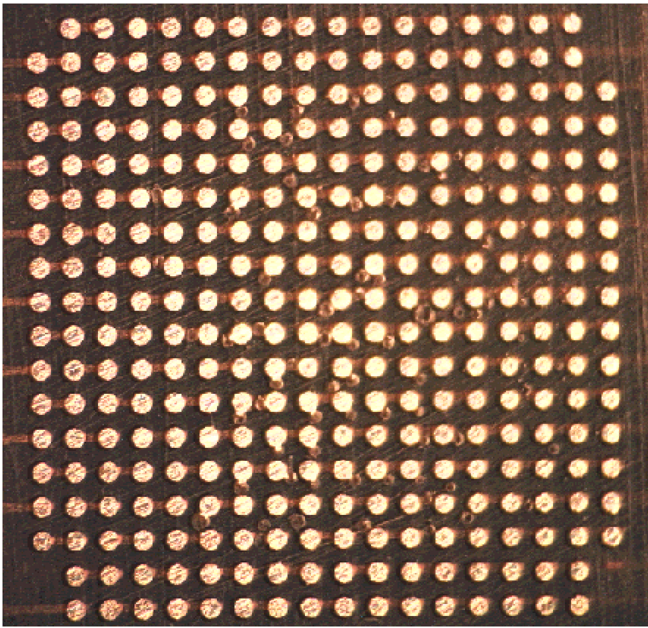

Figure 7. Underfill A, dot, speed 5 mm/s. Underfill voiding can be seen easily

Speed is a factor at .10 significance level for Underfill A and B. The difference in mean response for speed 1 and speed 2 was only about 20%. The relatively high p-value and the small difference in mean response led us to eliminate speed as a significant factor for further experiments.

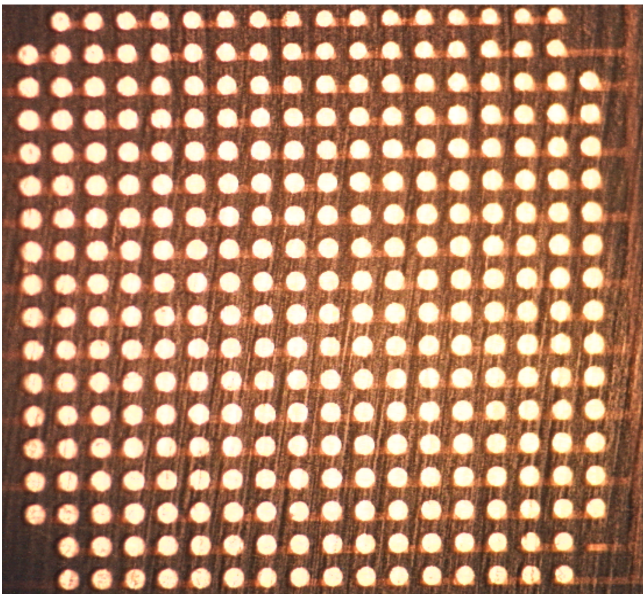

Figure 8. Underfill B, line, 70mm/s

DOE2

The only interconnect failures observed were for the 111 treatment (dot, 1N, 0 s). All materials show similar characteristics with respect to interconnect yield. All three placement parameters affect the response. The line pattern resulted in 100% yield for all materials regardless of the force or dwell used. This is interpreted as due to the relatively small force resulting from die placement onto the line pattern, rather than the full force from squeeze flow under the usual dot pattern placement. The F5 placement machine triggers the onset of dwell time after reaching the critical force of placement, and then after the dwell time has completed the chip is released. The line pattern evidently results in a placement force small enough that even with the machine dialed to 1N and no dwell time, the chip release is not triggered until the chip meets the board. When using the dot pattern with minimum force and no dwell, the die release must happen above the substrate resulting in misalignment after reflow and therefore a low percent interconnect yield. X-ray confirmed misalignment of those assembles that failed continuity testing.

Reflow

A material ranking was developed for each material based on the observable metrics: yield, underfill material voiding, resitance, and a grain size ratio. Data was collected for each material, an example is shown in Figure 9.

Material C	Voiding (% area)	Resistance (Ω)	Grain (ratio)	Ranking
Baseline	1.05	1.707	0.037	0.462
Rrhigh	0.828	1.714	0.043	0.437
Rrlow	0.675	1.713	0.044	0.480
SkTemphi	0.493	1.676	0.033	0.819
SkTemplow	0.863	1.677	0.028	0.746
SkTimehi	0.558	1.711	0.039	0.573
SkTimelow	1.085	1.726	0.053	0.207
T>183high	0.27	1.680	0.042	0.782
T>183low	0.68	1.705	0.059	0.373
PkTemphi	0.743	1.674	0.042	0.660
PkTemplow	1.553	1.662	0.038	0.501
Optimal	0.178	1.728	0.03	0.700

Figure 9. Material Ranking Data for Reflow Optimization

A weighted ranking system was chosen to place 40 percent weight on the underfill voiding data, and 30 percent each on the resistance and grain ratio data. The data for each material was scaled using the high and low values from each metric. This is shown in the following equation:

$$Rank = 0.4\frac{(V_{hi} - V)}{V_{hi} - V_{low}} + 0.3\frac{(R_{hi} - R)}{R_{hi} - R_{low}} + 0.3\frac{(G_{hi} - G)}{G_{hi} - G_{low}}$$

Where:
V = Voiding area as a percentage
R = Electrical resistance
G = Grain ratio

The voiding percent area was determined using the DIA software as in DOE1 and DOE2. The resistance data was taken by adding the resistance measurements from individual trace measurements for each die.

The grain data was determined using an area ratio technique, where a grid was overlaid onto SEM images and the ratio of points was calculated that fell inside of the large grain boundaries. See Figures 10 & 11.

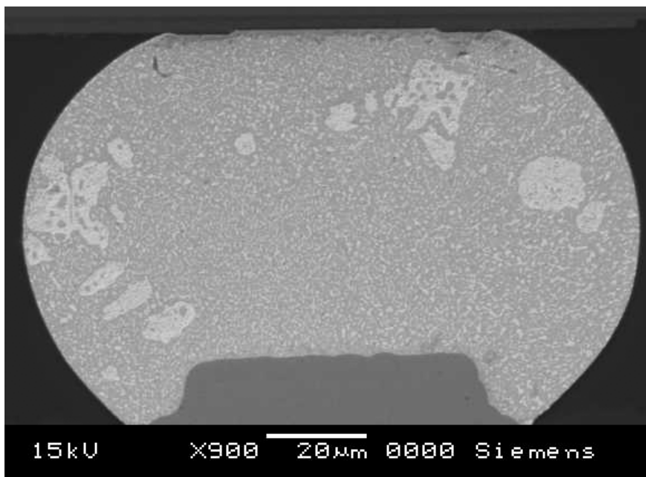

Figure 10. SEM Image of a cross section to be used for grain ratio analysis.

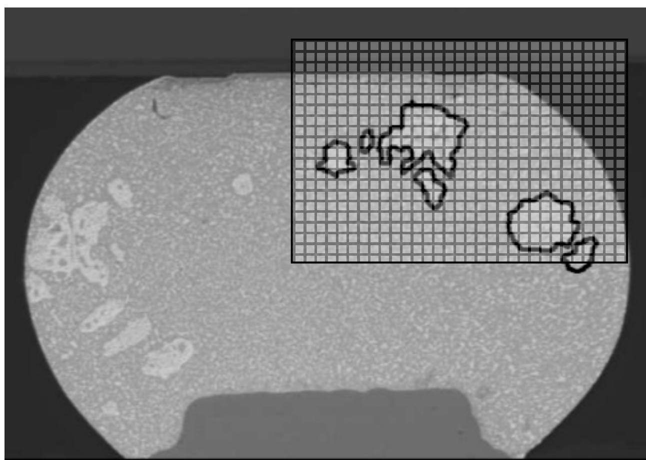

Figure 11. SEM Image with grain boundaries and a partial grid overlay.

The ranking in the provided 'Rank' equation gives a weighted score from 0 to 1, with the higher number corresponding to low values of voiding, resistance, and grain ratio.

For each material, the highest ranking profile was selected for use in the final reliability build of 30 replicates.

Reliability

A total of 120 samples, 4 underfill materials with 30 replicates each, have been subjected to air-air temperature cycle testing. The temperature cycle test ranged from -40°C to 125°C with 12 minute dwells at each temperature extreme. Assemblies built for final reliability testing have completed 2000 cycles thus far without an electrical failure. The parts will continue cycling in order to obtain failure data.

CONCLUSION

A near void free no flow underfill dispense process was developed including a novel ranking methodology for improved reflow process characterization. Test vehicles produced with this process have exhibited superior reliability performance – 2000 temperature cycles without an electrical failure.

ACKNOWLEDGEMENT

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