Electronics Components and Technology Conference
Seattle, WA, May 25-28, 1998

Thermal Dissipation Analysis in Flip Chip On Board and Chip On Board Assemblies

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Abstract

Direct chip attach packaging technologies are finding increasing application in electronics manufacturing particularly in telecommunications and consumer electronics. In these systems, bare die with bumped interconnect bond pads are assembled in a flip chip configuration (i.e., active face down) directly to low-cost organic substrates. In the current work, thermal management of three direct chip attach technologies is investigated. Experimental measurements are conducted exploring the junction-to-ambient thermal resistance and thermal dissipation paths for three interconnect technologies including solder attach, anisotropic adhesive attach, and isotropic adhesive attach. A first order chip-scale thermal design model is developed for flip chip assemblies exhibiting good agreement with the experimental measurements.

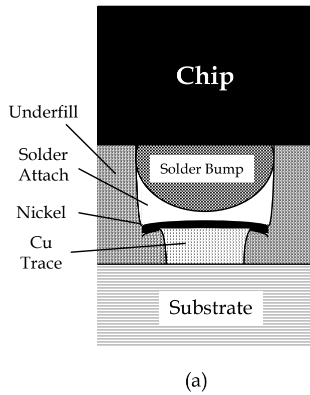
Introduction

Thermal management in business and consumer electronics is a persistent challenge as customers demand increased functionality, increased speed, reduced size, and reduced weight. These requirements increase power dissipation and raise circuit operating temperatures to limiting values. For example, in portable handheld products common problems include product returns, customer complaints, and warranty servicing resulting from product operating temperatures just a few tenths of a degree above normal body temperature. Unfortunately, the vastly different thermal dissipation characteristics of direct chip attach (DCA) assemblies over surface mount and through hole technology, makes the wealth of thermal performance data tabulated in recent years of little use in designing circuit packs having DCA. The ultimate goal of this work is to develop a thorough thermal performance characterization of DCA technologies and quantify these in terms of thermomechanical design guidelines. The focus on thermal management in still air environments has particular relevance for handheld portable electronics, which are driving DCA technologies. The objectives is this work are to characterize the thermal dissipation in direct chip attach (DCA)/flip chip on board (FCOB) assemblies, evaluate thermal performance of select DCA interconnect technologies, and develop and verify a DCA thermal management design model for rapid evaluation. A portion of this work was originally published in the 1996 International Mechanical Engineering Congress and Exposition [1].

In direct chip attach assembly technologies, bare chips with bumped interconnect bond pads are assembled in a flip chip configuration directly to low-cost organic substrates. In this work, the thermal management of three DCA technologies is investigated including solder attach, anisotropic conductive adhesive attach, and isotropic conductive adhesive attach. Experimental measurements of junction-to-ambient thermal resistances and temperature profiles along the primary thermal dissipation paths are performed. A first order chip-scale thermal design model is developed for flip chip assemblies. Comparison of model predictions and experimental measurements indicates good agreement.

There are numerous interconnect materials and technologies available for flip chip assembly. Three major systems are shown in Figure 1. The first is solder attach interconnection, introduced by IBM as the controlled collapse chip connection (C4) for high melting point solders [2,3] and more recently adapted for lower melting point eutectic solder. A variant of this technique uses eutectic solder to form an interconnection to a high melting point solder bump on the chip as shown in Figure 1a [4]. Subsequent to reflow, the solder attach system is underfilled with a silica filled epoxy and cured. Anisotropic conductive adhesives are also being investigated for flip chip interconnect materials where z-axis-conductive, pressure-sensitive tapes and/or pastes are used to form the I/O interconnections and supply mechanical coupling between the chip and substrate (similar to underfill) [5]. Isotropic conductive adhesives are also being investigated for flip chip applications [6,7]. With these materials, isotropically conductive adhesive, typically an epoxy loaded with silver flakes, is used to locally interconnect the I/O of the bumped chip to the substrate traces. In this case, the device is underfilled using standard encapsulant underfills.

Baldwin et al. [1] presented one of the first studies of thermal management for low cost direct chip attach assembly technologies to low cost organic substrates. Zhou et al. [8] presented a recent thermal study of flip chip on board technology investigating the effect of die and substrate configurations, underfill material, and heat sink applications. A thermal characterization of electrically conductive adhesive bumps is presented by Sathe et al. [9]. In that study a three-dimensional heat transfer model is developed for a card assembly based on a finite volume technique showing good agreement with experimental measurements. Early work in thermal management on flip chip assemblies concentrated on controlled collapse chip connection (C4) technology, where the die is mounted on higher cost ceramic substrates, and



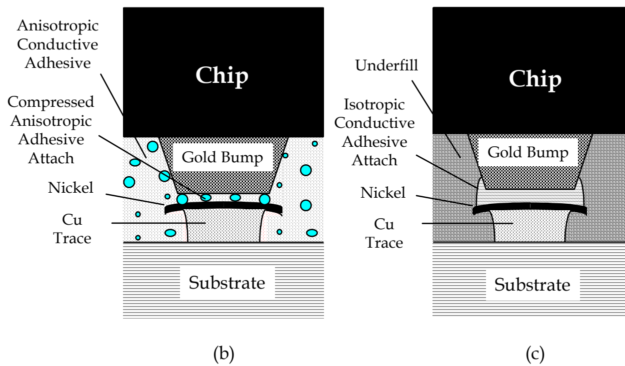


Figure 1: Primary interconnect technologies for direct chip attach assemblies. (a) solder attach, (b) anisotropic adhesive attach, and (c) isotropic adhesive attach.

multi-chip modules. While the studies conducted in these two arenas are too numerous to list here, a representative thermal management study is presented by Lee et al. [10].

Test Vehicles

The test vehicles utilized in this project were designed based on an assembly test chip developed by Sandia National Laboratories: assembly test chip version 04 (ATC04) [11]. Thermal evaluation of electronic assemblies and packages is commonly performed using test chips [12]. In order to reasonably mirror portable product applications, epoxy glass substrates (FR4) 0.8 mm (32 mils) thick were chosen. The glass transition temperature of the FR4 substrates was approximately 130°C. The trace specifications were one ounce copper, plated with 3 μm (125 μ-inch) nickel and 0.5 to 0.7 μm (20 to 30 μ-inch) gold. In all cases, the printed wiring boards (PWBs) were single layer with separate designs for the chip-on-board test vehicles and flip chip test vehicles.

The ATC04 is a CMOS device designed to measure mechanical stress and thermal resistance [11]. Each device is 5.8 mm square (228 mils) and has 108 perimeter I/O on a pitch of 185 μm (7.28 mils) with silicon nitride passivation. The passivation openings over each pad are 90 μm (35.4 mils) square. The ATC04 contains two ring oscillators with typical operating frequencies of 20 MHz (M1) and 45 MHz (M2). The ring oscillators are used to monitor the general health of the integrated circuit (IC). The ATC04 operates at 5 volts, and all required bond pads are replicated on each of the four sides of the chip. The chip layout includes an array of 25 test cells each containing eight piezoresistor stress sensors and a temperature sensitive diode. The test cell piezoresistors and

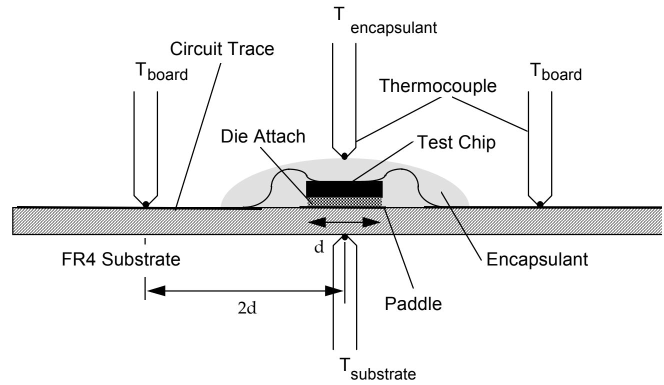


Figure 2: Typical configuration of thermal management wire bond test vehicles during thermal resistance tests.

diode can be addressed independently via a nine bit address bus. Temperature and stress measurements are made using a four point technique. The ATC04 also contains four independent polysilicon heater elements with approximate resistances of 20Ω.

Figure 2 illustrates the configuration of the chip on board (COB) thermal management test vehicles. The ATC04 was attached to the FR4 substrate using a silver filled epoxy die attach (Ablestik, Ablebond 8380). The I/O interconnections were formed by aluminum wire wedge bonding using a Hughes Model 2470-III wedge bonder. Samples were tested with and without "glob-top" encapsulant (Dexter Hysol 4402). Four 36 gage type K thermocouples were mounted to the test vehicles to monitor the "substrate" temperature directly under the chip, the "board" temperature at twice the chip dimension from the test vehicle center, and the "chip" and/or "encapsulant" temperature as shown in Figure 2.

The configuration of the flip chip thermal management test vehicles is illustrated in Figure 3. For the anisotropic adhesive attach interconnects (see Figures 1b and 3), the ATC04 device was gold wire stud bumped using a Hughes Model 2460-IV thermosonic wirebonder and 25 μm (1 mil) gold wire. Hitachi AC8201x anisotropic conductive film was selected as the interconnect and attachment material with an approximate thickness of 50 μm (2 mils). The chip, substrate, and adhesive were aligned and tacked in a Semiconductor Equipment Corporation (SEC) bonder model 4150. The tack

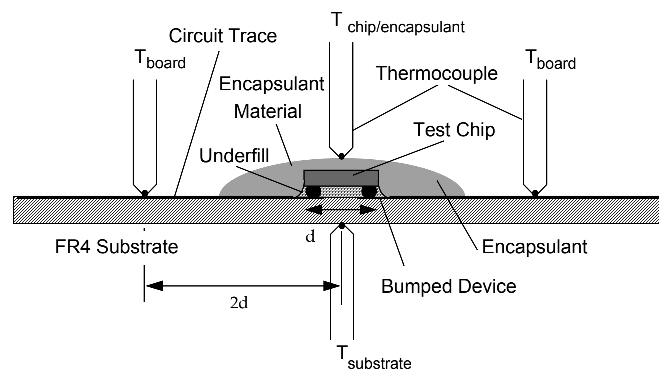


Figure 3: Typical configuration of thermal management flip chip test vehicles during thermal resistance tests.

bonding conditions were a bond load = 100 g, collect temperature = 145°C, stage temperature = 35°C. A secondary high pressure and temperature process was used to cure the adhesive interconnect and bond the test vehicles. Using a precision alignment fixture mounted in a temperature controlled press, the test vehicles were bonded at a load of 10 pounds at a temperature of 175°C for 5 minutes. Samples were tested with and without glob-top encapsulant (Dexter Hysol FP4402).

The isotropic adhesive attach interconnects were assembled as shown in Figure 1c and 3. Here an isotropic conductive adhesive (Ablebond Ablestik 8175A) was stencil printed (using a 50 μm stencil with 100x150 μm apertures) onto the traces of an FR4 substrate. A gold wire stud bumped ATC04 was then aligned and bonded to the substrate using the SEC bonder. The adhesive was cured in situ at a load of 100 g and a collect temperature of 160°C for 5 minutes. Post cure, underfill encapsulant (Dexter Hysol FP4511) was applied under the device and tack-cured under the collet load at a temperature of 160°C for one hour. The assembly was cooled and removed from the bonder. The final cure of the samples was accomplished in a forced convection oven at 150°C for one hour. Samples were tested with and without glob-top encapsulant (Dexter Hysol FP4402).

The final interconnect system studied was a solder attach system shown in Figures 1a and 3. The devices were first gold wire stud bumped using 25 μm gold wire. The bumped devices were attached to FR4 substrates using 60/40 tin/lead solder. To form robust interconnects, Kester R244 type five solder paste was printed on a glass panel using a 50 μm stencil with 75x125 μm apertures. The gold bumped ATC04s were then aligned to the printed solder and placed on the glass panel using a MRSI flip chip bonder at a bond load of 500 g, collet temperature of 25°C, and a stage temperature of 25°C. The solder was transferred to the gold bumps during reflow on a programmable strip heater in a nitrogen atmosphere at 210 °C over a 16 sec profile. While the gold-tin intermetallics formed during reflow are of a concern for long term interconnect reliability, this was not considered relevant in this study since thermal dissipation was the focus, not reliability. Once cleaned, the devices were aligned and bonded to the FR4 substrates using the MRSI bonder at a bond load of 500 g, collet temperature of 25°C, and a stage temperature of 25°C. The assemblies were fluxed and reflowed on a programmable strip heater in a nitrogen environment at 200 °C for 10 sec. Dexter Hysol FP4511 underfill was applied under the devices at a temperature of 90 °C. The assemblies were cured in a forced convection oven at 150 °C for two hours.

Chip Scale Thermal Design Model

To model the thermal dissipation of flip chip assemblies, a relatively simple first order thermal resistance network was formulated (i.e., the chip scale thermal design model). The primary intent of this model was to formulate a design model allowing rapid evaluation of thermal performance characteristics in new interconnect technologies. The objectives of this modeling work were to estimate the temperature profiles along the primary thermal dissipation paths, the effective thermal resistances of the primary thermal dissipation paths, and the junction-to-ambient thermal resistances of DCA assemblies. The general thermal resistance network utilized is shown in Figure 4. In the chip scale thermal model, the heat source is approximated as a point source represented by an equivalent junction, at a junction temperature, T_j, comprising the average power dissipated across the device.

The heat generated at the junction is modeled as having three primary paths to reach ambient. The first is conduction through the silicon chip and convection from the back side of the chip to ambient. The second is conduction through the interconnect system including the bumps and interconnect attach and combined conduction/convection from the substrate traces to the ambient. The final thermal dissipation path is conduction through the underfill and combined conduction/convection from the base substrate (FR4) to ambient. Secondary heat transfer paths are assumed negligible in this analysis. As a first order approximation, radiation heat transfer is neglected in this analysis. In its simplest form, the junction-to-ambient thermal resistance is given by equation (1) based on Figure 4.

$$\frac{1}{R_{\theta ja}} = \frac{1}{R_{Si}^{cond} + R_{chip}^{conv}} + \frac{1}{R_{bump}^{cond} + R_{attach}^{cond} + R_{trace}^{eqv}} + \frac{1}{R_{underfill}^{cond} + R_{substrate}^{eqv}} \tag{1}$$

The junction temperature can then be estimated from equation (2).

$$T_j = T_a + qR_{\theta ja} \tag{2}$$

where T_j is the junction temperature, T_a is the ambient temperature, q is the total power input, and $R_{\theta ja}$ is the junction-to-ambient thermal resistance. Similar expressions can be derived to estimate the temperature profiles along the three primary heat transfer paths.

The thermal resistances for the elements experiencing pure conduction are calculated using a simple lump resistance

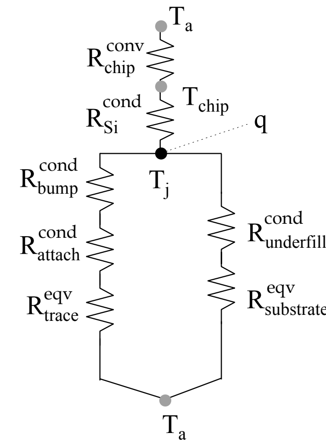


Figure 4: Thermal resistance network for chip scale thermal model.

model with the average resistance given by

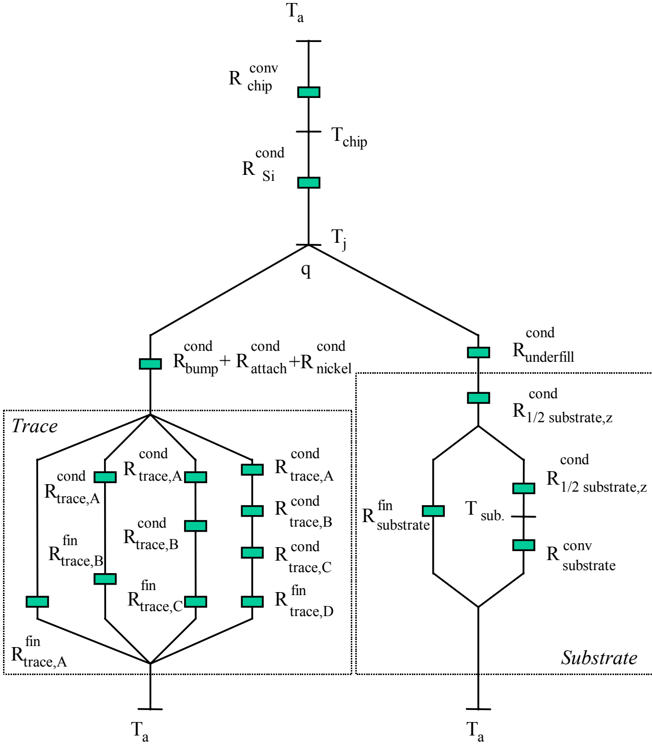


Figure 5: Complete thermal resistance network for the chip scale thermal design model.

$$R_i^{cond} = \frac{L_i}{k_i A_i} = \frac{L_i}{k_i (W_i H_i)} \tag{3}$$

where L is the conduction length, k is the thermal conductivity, and A is the cross-sectional area through which conduction heat transfer occurs. The subscript i corresponds to the various elements for which conduction is the primary heat transfer mechanism: i = Si (silicon), bump, attach, underfill, substrate along z-axis (thickness direction).

Since all of the heat in an electronic package is eventually dissipated into the air by convection, a convection coefficient, h, is needed for the substrate, traces, and chip. For the still air analysis and experiments forming the focus of this work, free convection is used to model the heat transfer from the exposed surfaces. The average convection heat transfer coefficient can be estimated from the average Nusselt number, $\overline{Nu}_L$.

$$h = \frac{k}{L}\overline{Nu}_L \tag{4}$$

where k is the thermal conductivity of the convection medium and L is the characteristic length of the convection surface given by the ratio of surface area to wetted perimeter. Empirical correlations for horizontal flat plates yield average Nusselt numbers for plates of characteristic length L given by equations (5) and (6) [13].

$$\overline{Nu}_L = 0.54 Ra_L^{1/4} \tag{5}$$

$$\overline{Nu}_L = 0.27 Ra_L^{1/4} \tag{6}$$

Equation (5) is for the upper surface and equation (6) is for the lower surface. Ra_L is the Rayleigh number and given by

$$Ra_L = \frac{g\beta(T_s - T_a)L^3}{\nu\alpha} \tag{7}$$

where g is gravitational acceleration, β is the volumetric expansion coefficient which modeling air as an ideal gas equals the inverse of the air temperature $\left(1/T \approx 1/T_f = 2/(T_s - T_a)\right)$, T_s is the average surface temperature, L is the characteristic length of the plate given by a surface area to wetted parameter ratio, υ is the viscosity of air, and α is the thermal diffusivity of air.

The simplest utilization of the convection coefficient is to estimate convection heat transfer from the back of the chip. Its thermal resistance is estimated from

$$R_{chip}^{conv} = \frac{1}{h_{chip} A_{chip}} \tag{8}$$

where h_{chip} is the convection heat transfer coefficient for the backside of the chip and A_{chip} is the x-y plane cross-sectional area of the device. Similarly, the convection heat transfer from the substrate localized directly under the chip on the underside of the substrate, can be estimated by equation (9).

$$R_{substrate}^{conv} = \frac{1}{h_{substrate} A_{chip}} \tag{9}$$

In addition to convection off the back of the chip and localized substrate convection, the combined conduction/convection heat transfer from the substrate and the traces must be estimated. Looking at the traces, the equivalent thermal resistance is represented by the thermal resistance network in Figure 5. For the particular test vehicles used in the experimental study, the traces were staged in four increasing line widths (i.e., $W_{trace,A}$, $W_{trace,B}$, $W_{trace,C}$, $W_{trace,D}$) from 100 μm (4 mils) to 127 μm (50 mils). To effectively account for this thermal resistance, four parallel heat transfer paths are modeled, each allowing for fin analysis along a single stage of the trace. In this case, the geometric complexity demands that each geometrically equivalent stage of the traces be analyzed independently. The combined conduction/convection heat transfer for a particular stage (i.e., width) of the trace is modeled using fin analysis. The previous stages of the traces are modeled as series resistances representing the conduction thermal resistance through each stage. The equivalent resistance of a single trace is given by equation (10).

$$\begin{aligned}\frac{1}{R_{trace}} = &\frac{1}{R_{trace,A}^{fin}} + \frac{1}{R_{trace,A}^{cond} + R_{trace,B}^{fin}} \\ &+ \frac{1}{R_{trace,A}^{cond} + R_{trace,B}^{cond} + R_{trace,C}^{fin}} \\ &+ \frac{1}{R_{trace,A}^{cond} + R_{trace,B}^{cond} + R_{trace,C}^{cond} + R_{trace,D}^{fin}}\end{aligned} \tag{10}$$

where the subscripts A, B, C, and D represent the four sequential stages of a trace. The total equivalent resistance for all of the trace resistances, which are in parallel, is

$$R_{trace}^{eqv} = \frac{R_{trace}}{n} \quad (11)$$

where n is the number of I/O on the flip chip device (i.e., number of traces).

To approximate the equivalent substrate resistance, the complicated geometry of the substrate is modeled to allow for heat conduction through half of the substrate thickness (equation 3). As shown in Figure 5, parallel heat transfer paths exist from this point to ambient. The substrate itself acts like a fin allowing for both conduction and convection heat transfer. The remainder of the heat conducts through the second half of the substrate thickness and allows for convection from the bottom side of the substrate directly under the chip (equations 3 and 5, respectively). The equivalent thermal resistance of the substrate is given by:

$$R_{substrate}^{eqv} = R_{1/2substrate,z}^{cond} + \left(\frac{1}{R_{substrate}^{fin}} + \frac{1}{R_{1/2substrate,z}^{cond} + R_{substrate}^{conv}} \right)^{-1} \quad (12)$$

Fin analysis is used to model the thermal resistance of the traces and the substrate,. In general, the temperature profile along a fin is given by a second order differential equation (Incropera and DeWitt, 1990).

$$\frac{d}{dx}\left(A_c \frac{dT}{dx} \right) - \frac{h}{k}\frac{dA_s}{dx}\left(T - T_a \right) = 0 \quad (13)$$

where A_c is the cross-sectional area through which heat conducts, A_s is the surface area of the fin, and h is the convection coefficient. This differential equation was simplified for the trace and board accounting for the appropriate cross-sectional and surface areas. Equation 14 represents the fin heat transfer rate of each section of the trace, where $m = (hP/kA_c)^{1/2}$, h is the convection heat transfer coefficient, P is the wetted parameter exposed to air, k is the thermal conductivity of the trace material, A_c is the cross-sectional area, T_b is the base temperature of the trace, and T_a is the ambient temperature. In this analysis, the tip of the fin was approximated as adiabatic.

$$q_f = \sqrt{hPkA_c}\left(T_b - T_a \right)\tanh mL \quad (14)$$

The equivalent thermal resistance for the trace experiencing combined conduction and convection is then:

$$R_{trace,i}^{fin} = \frac{q_f}{T_b - T_a} = \sqrt{hPkA_c}\ \tanh(mL) \quad . \quad (15)$$

In order to model the combined conduction/convection heat transfer from the substrate, it is approximated as a radial fin with a single vane. Equation 16 approximates the fin heat transfer rate of the substrate, where r_b is the effective radius to the base of the substrate fin section, r_e is the effective radius to the edge of the substrate, t is the substrate thickness, k is the thermal conductivity in the plane of the substrate, T_b is the base temperature of the substrate, T_a is the ambient temperature, $n = (2h/kt)^{1/2}$, and K_1, K_0, I_1, and I_0 are Bessel functions [14]. In this analysis, the substrate is treated as an annular fin having an internal effective radius of r_b and an outer effective radius of r_e. The effective radii are calculated based on equivalent wetted area for the actual substrate and the annular fin approximation.

$$q_f = \left((2\pi)ktnr_b \right)\left(T_b - T_a \right)\left(B \right) \quad (16)$$

where $$B = \left[\frac{K_1(nr_b)I_1(nr_e) - I_1(nr_b)K_1(nr_e)}{K_0(nr_b)I_1(nr_e) - I_0(nr_b)K_1(nr_e)} \right]$$

The equivalent thermal resistance for the substrate experiencing combined conduction and convection is then

$$R_{substrate}^{fin} = \frac{q_f}{T_b - T_a} = \frac{(2\pi)ktnr_b}{B} \quad (17)$$

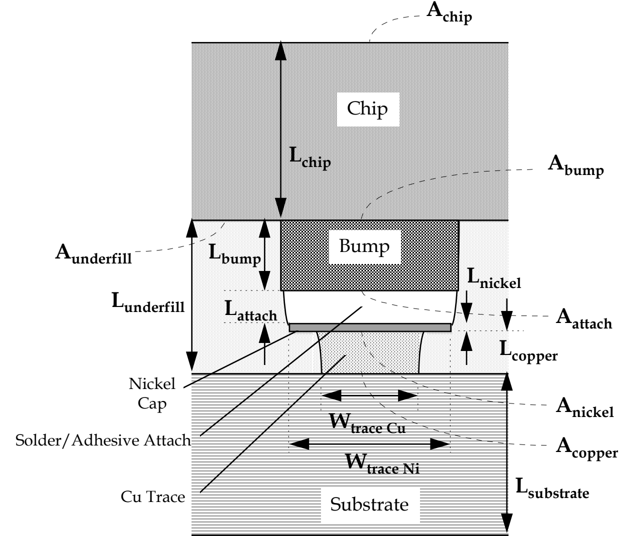


Figure 6: Schematic of interconnect geometry for chip scale thermal model.

The chip scale thermal model parameters consist of the thickness, widths, lengths, thermal conductivities, and areas of the different areas of the DCA assembly, and are given in Table 1 for the test vehicles used in the experimental study. A schematic of the interconnect geometry identifying the specific modeling parameters is illustrated in Figure 6. The heat transfer model presented above was implemented on a commercial spreadsheet to allow rapid evaluation of thermal performance in DCA assemblies.

Experimental Procedures

Experimental characterization of the DCA thermal management test vehicles was based on junction-to-ambient thermal resistance tests in still air following SEMI specification G38-87 [15]. By definition, the thermal resistance of a microelectronic device is a measure of the device, package, or assembly's ability to dissipate heat to a reference environment. The junction-to-ambient thermal resistance is a primary thermomechanical design metric needed for package selection and circuit board layout. The relationship used to calculate the junction-to-ambient thermal resistance is given by equation (18) where T_a is the ambient temperature and P_H is the total dissipated power.

$$R_{\theta ja} = \frac{\left(T_j - T_a \right)}{P_H} \quad (18)$$

Calculation of the thermal resistance requires a known semiconductor junction temperature, T_j (i.e., the internal device operating temperature). In this study, the junction

Table 1: Nomenclature and chip scale thermal design model parameters.

Model Parameter	Description	Test Vehicle Parameters	Solder Attach Parameters	Anisotropic Adhesive Attach Parameters	Isotropic Adhesive Attach Parameters
n	number of traces on board		108	108	108
L_{bump}	thickness of gold bump		37.6 µm	37.6 µm	37.6 µm
K_{bump}	thermal conductivity of gold bump		317 W/mK	317 W/mK	317 W/mK
A_{bump}	planar area of one gold bump		0.0081 mm^2	0.0081 mm^2	0.0081 mm^2
L_{attach}	thickness of bump attachment		13.9 µm	8 µm	12 µm
K_{attach}	thermal conductivity of bump attachment		22 W/mK	2 W/mK	2.7 W/mK
A_{attach}	area of attachment in contact with bump		0.0081 mm^2	0.0081 mm^2	0.0081 mm^2
L_{nickel}	thickness of nickel on trace		6.66 µm	6.66 µm	6.66 µm
K_{nickel}	thermal conductivity of nickel		90 W/mK	90 W/mK	90 W/mK
A_{nickel}	area of nickel in contact with attach		0.0081 mm^2	0.0081 mm^2	0.0081 mm^2
$W_{trace,A\ Ni}$	width of nickel of trace A		102 µm	102 µm	102 µm
$W_{trace,B\ Ni}$	width of nickel of trace B		153 µm	153 µm	153 µm
$W_{trace,C\ Ni}$	width of nickel of trace C		510 µm	510 µm	510 µm
$W_{trace,D\ Ni}$	width of nickel of trace D		1300 µm	1300 µm	1300 µm
$W_{trace,A\ Cu}$	width of copper of trace A		52 µm	52 µm	52 µm
$W_{trace,B\ Cu}$	width of copper of trace B		103 µm	103 µm	103 µm
$W_{trace,C\ Cu}$	width of copper of trace C		460 µm	460 µm	460 µm
$W_{trace,D\ Cu}$	width of copper of trace D		1250 µm	1250 µm	1250 µm
$L_{trace,A}$	average length of trace A		3.4 mm	3.4 mm	3.4 mm
$L_{trace,B}$	average length of trace B		12.3 mm	12.3 mm	12.3 mm
$L_{trace,C}$	average length of trace C		33 mm	33 mm	33 mm
$L_{trace,D}$	average length of trace D		10 mm	10 mm	10 mm
L_{copper}	thickness of copper of trace		66.7 µm	66.7 µm	66.7 µm
K_{copper}	thermal conductivity of copper		390 W/mK	390 W/mK	390 W/mK
$L_{underfill}$	thickness of underfill		104 µm	104 µm	104 µm
$K_{underfill}$	thermal conductivity of underfill		0.054 W/mK	0.65 W/mK	0.054 W/mK
$A_{underfill}$	area of underfill in contact with chip		33.6 mm^2	33.6 mm^2	33.6 mm^2
$L_{1/2\ substrate}$	half the thickness of board		406.5 µm	406.5 µm	406.5 µm
$K_{board\ x\text{-}y}$	board thermal conductivity x-y direction		0.9 W/mK	0.9 W/mK	0.9 W/mK
$K_{substrate,z}$	board thermal conductivity z direction		0.9 W/mK	0.9 W/mK	0.9 W/mK
$L_{substrate,z}$	thickness of substrate		813 µm	813 µm	813 µm
r_b	effective "radius" of chip		3 mm	3 mm	3 mm
r_e	effective radius on substrate, 1.5*L_{chip}		50 mm	50 mm	50 mm
A_{chip}	area of chip		33.6 mm^2	33.6 mm^2	33.6 mm^2
L_{chip}	thickness of chip		660 µm	660 µm	660 µm
$K_{silicon}$	thermal conductivity of silicon		148 W/mK	148 W/mK	148 W/mK
$K_{soldermask}$	thermal conductivity of solder mask		0.21 W/mK	0.21 W/mK	0.21 W/mK

Table 2: Average junction-to-ambient thermal resistances for three dca interconnect technologies.

Interconnect	*Experimental @ 1 W*	*Experimental @ 0.1 W*	*Predicted @ 1 W*	*Predicted @ 0.1 W*
Solder Attach	80 °C/W	84 °C/W	78 °C/W	99 °C/W
Isotropic Adhesive Attach	71 °C/W	87 °C/W	80 °C/W	101 °C/W
Anisotropic Adhesive Attach	62 °C/W	69 °C/W	76 °C/W	97 °C/W
Chip on Board	87 °C/W	88 °C/W		

Table 3: comparison of the experimental and predicted temperature profile for the solder attach flip chip test vehicles at 0.1 and 1.02 W power dissipation.

Power Dissipation (W)		Ambient (C)	Junction (C)	Chip (C)	Board (C)	Substrate (C)
0.10	Experimental	22.0	32.0	31.0	21.0	30.0
0.10	Model	22.0	32.0	32.0	25.0	30.0
	Predicted Accuracy (%)		1	2	18	1
1.02	Experimental	23.0	107	105	47.0	93.0
1.02	Model	23.0	102	101	42.0	86.0
	Predicted Accuracy (%)		5	4	11	8

voltage (V_{be}) in the ATC04 test cells. A schematic of the ATC04 test die is shown elsewhere [11]. The diode voltage is a temperature sensitive parameter (TSP) having a known calibration [11]. The junction temperature is calculated using equation (19) where T_{a0} is the ambient temperature of the baseline (or reference) measurement, V_{be} is the diode voltage from the four point measurement, V_{be0} is the diode voltage of the baseline (or reference) measurement, and $(dT/dV_{be})_{cal}$ is the TSP calibration factor equaling -544 °C/V [11].

$$T_j = T_{a0} + \left(V_{be} - V_{be0}\right)\left(\frac{dT}{dV_{be}}\right)_{cal} \quad (19)$$

The thermal resistance values are based on the junction temperature rise over a specified reference temperature (i.e., ambient, case, substrate, etc.) normalize with respect to the power dissipated by the device. In general, the device power, P_H, is equal to the power dissipated in the four polysilicon heaters, R_{HTRi}. The resistances of the polysilicon heaters for each test vehicle were measured prior to the experiments and ranged in value from 21 to 24 Ω. The automated testing system was used to monitor the current supplied to the heaters via the voltage, V_{Ri}, across calibrated series resistors, R_i having resistances of R_1=10.149 Ω, R_2=10.187 Ω, R_3=10.135 Ω, and R_4=10.089 Ω. The total dissipated power, P_H, was controlled by a regulated voltage supply and was calculated using equation (20).

$$P_H = \sum_{i}^{4} R_{HTRi}\left(V_{Ri}/R_i\right)^2 \quad (20)$$

The thermal resistance measurements were performed over a 16 hour period to insure steady state operation. The measurements of the forward bias diode voltage, V_{be}, were performed using a four point technique at an applied current of 100 μA. An automated testing system based on the Labview platform was used to control the data acquisition system which recorded the forward bias diode voltage, V_{be}, the ring oscillator frequencies (M1 and M2), and the series resistor voltages for the heater circuits, V_i. Each test vehicle had four type K thermocouples mounted to it as shown in Figures 2 and 3. These thermocouples measured the ambient air temperature, the chip or encapsulant temperature on the back of the chip, the substrate temperature directly under the chip, and the board temperature at a distance twice the characteristic chip dimension from the test vehicle center. For each test vehicle, over 180 data samples were taken for each parameter over the 16 hour testing period and the steady state values averaged. Still air thermal resistance measurements were performed for all of the test vehicle configurations. Four test vehicles were assembled for each interconnect configuration (solder attach, isotropic adhesive attach, anisotropic adhesive attach) and encapsulant configuration (with glob top and without glob top). The data reported represent the average of the four measurements in each case.

Results and Discussion

Junction to Ambient Thermal Resistance Measurements

Figure 7 shows the junction-to-ambient thermal resistance values measured. The data includes the COB wire bond control samples (with and without encapsulant), the anisotropic adhesive attach samples (with and without encapsulant), the isotopic adhesive attach samples (with and without encapsulant), and the solder attach samples (without encapsulant). The solid trendlines represent the glob top encapsulated test vehicles while the dashed trendlines represent the test vehicles without glob top. It is important to keep in mind that the $R_{\Theta ja}$'s reported in Figure 7 are on the conservative side in that the test vehicles did not incorporate

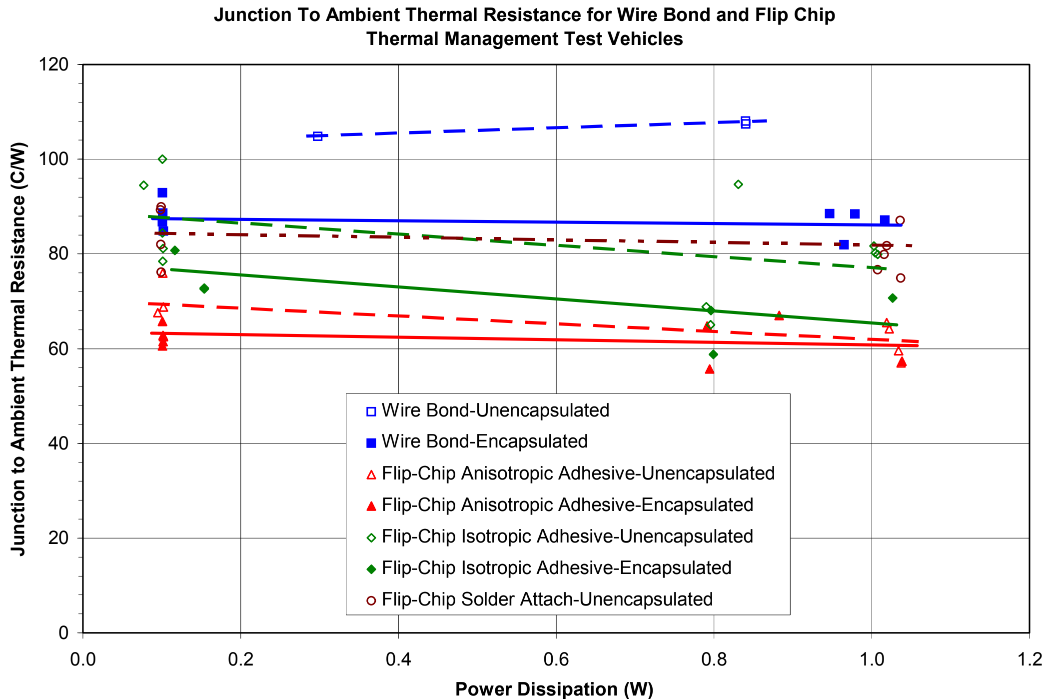


Figure 7: Junction-to-ambient thermal resistance measurements for the thermal management test vehicles including wire bond attach, anisotropic adhesive attach, isotropic adhesive attach, and solder attach.

Table 4: Comparison of the experimental and predicted temperature profile for the isotropic adhesive attach flip chip test vehicles at 0.1 and 1 W power dissipation.

Power Dissipation (W)		Ambient (C)	Junction (C)	Chip (C)	Board (C)	Substrate (C)
0.10	Experimental	24.0	32.0	32.0	26.0	31.0
0.10	Model	24.0	34.0	34.0	27.0	32.0
	Predicted Accuracy (%)		7	6	1	3
1.00	Experimental	23.0	104	104	47.0	93.0
1.00	Model	23.0	102	102	42.0	86.0
	Predicted Accuracy (%)		1	2	10	8

multi-layer boards, thermal vias, or other design features which promote heat spreading and low thermal resistances. In general, Figure 7 indicates that the junction-to-ambient thermal resistance decreases with device power. The chip scale thermal design model also predicts this result. The highest thermal resistance is exhibited by the COB assemblies without encapsulant having a $R_{\Theta ja}$ up to 110°C/W. The lowest thermal resistance measured was for the encapsulated anisotropic adhesive attach assemblies having an $R_{\Theta ja} \approx$ 62°C/W. The limited data available for flip chip packaging suggests typical still-air thermal resistances between 15 to 30°C/W. This is considerably lower than the values reported in Figure 7. This is believed to result from the inclusion of design features to enhance thermal dissipation (such as multi-layer boards and thermal vias) in the latter. Based on these results, it is clear that the flip chip configuration provides for more efficient thermal dissipation then the COB configuration.

Figure 7 also demonstrates the importance of encapsulation for thermal dissipation purposes in still air environments. The encapsulated COB samples have a 23% lower thermal resistance than samples without encapsulation. The flip chip attach test vehicles also exhibited enhanced thermal dissipation with encapsulation. The effectiveness of the encapsulant is two-fold. First, it serves as a heat spreader thereby increasing the effective heat transfer area in contact with the die. Second, it provides for a more efficient heat flux path to the circuit traces and substrate, which reduces the thermal resistance. The encapsulated flip chip test vehicles showed a lesser impact on thermal resistance with the encapsulated test vehicles having a moderate 6 % decrease.

A significant finding of this work is the relatively low thermal resistance of the anisotropic conductive adhesive interconnect some 42 % lower than the encapsulated COB samples. Conversely, the isotropic adhesive attach assemblies have thermal resistances ranging between 15 and 24 % lower than the encapsulated COB samples. The solder attach assemblies exhibit a 5 to 8 % improvement in thermal performance over the encapsulated COB. The relatively poor performance of the solder attach assemblies is attributed primarily to numerous solder starved interconnects that resulted from the specific assembly process used. Under optimum assembly conditions, the thermal resistance of the solder attach assemblies is expected to be improved. It is believed that the lower resistance of the anisotropic assemblies results from the lower standoff of this attachment technique (e.g., the anisotropic adhesive had a 37 µm standoff while the isotropic adhesive and solder had a 87 µm standoff) and the enhanced thermal conduction of the anisotropic film as an underfill over the silica filled underfill material used for the other interconnects studied.

Figure 7 indicates considerable scatter in the thermal resistance data. The scatter was particularly large for the isotropic adhesive test vehicles. Scatter in the thermal resistance measurements is influenced in two ways; 1) by the inherent variations from sample to sample due to assembly variations such as underfill amount, standoff, void inclusions, encapsulant amount, interconnect variations, interconnect yield, etc, and 2) by the failure of interconnects during testing. Both occurred to varying degrees in this experimental study. For example, preliminary C-mode scanning acoustic microscopy (C-SAM) analysis of the samples indicates significant void formation in the anisotropic adhesive attach and solder attach test vehicles. In future studies, the impact of process induced defects will be studied to determine its

Table 5: Comparison of the experimental and predicted temperature profile for the anisotropic adhesive attach flip chip test vehicles at 0.1 and 1 W power dissipation.

Power Dissipation (W)		Ambient (C)	Junction (C)	Chip (C)	Board (C)	Substrate (C)
0.10	Experimental	21.0	28.0	28.0	24.0	28.0
0.10	Model	21.0	31.0	31.0	25.0	31.0
	Predicted Accuracy (%)		10	9	3	10
1.00	Experimental	22.0	86.0	88.0	43.0	80.0
1.00	Model	22.0	98.0	97.0	44.0	94.0
	Predicted Accuracy (%)		13	11	2	17

Table 6: Primary thermal resistance paths predicted by chip scale thermal model at 1 W.

Interconnect Material	*Flip Chip Thermal Dissipation Path* Chip $R^{conv}_{chip} + R^{cond}_{Si}$	Substrate $R^{cond}_{underfill} + R^{eqv}_{substrate}$	Interconnect System $R^{cond}_{bump} + R^{cond}_{attach} + R^{eqv}_{trace}$
Solder	4280 °C/W	344 °C/W	103 °C/W
Anisotropic Adhesive	4290 °C/W	289 °C/W	106 °C/W
Isotropic Adhesive	4260 °C/W	344 °C/W	107 °C/W

impact on thermal characteristics of flip chip assemblies.

Based on this rank ordering, some general thermomechanical design guidelines can be proposed. For single layer PWBs with equivalent I/O trace configurations, the results suggest a maximum allowable device power of 1.61 W for the anisotropic flip chip assembly and 1.13 W for the encapsulated COB assemblies[1]. These correspond to power dissipation densities of 4.8 W/cm^2 and 3.4 W/cm^2 for the anisotropic adhesive interconnects DCA assemblies and the encapsulated chip on board assemblies, respectively. COB assemblies should be encapsulated with a silica filled epoxy (or preferably a thermally conductive glob top material) to promote heat dissipation. This recommendation stems form the results comparing the encapsulated and unencapsulated chips. The device standoff should be minimized within limits feasible for reliability to promote low thermal resistances. Based on limited cross section analysis, it appeared that the assemblies with lower standoff heights tended to have lower thermal resistances. Multi-layer FR4 substrates with power and ground planes should be used to promote heat spreading and dissipation over a larger surface area and to minimize hot spots. Care should be taken to eliminate the formation of voids in the interconnect system. For example, voids should be minimized in the underfill/encapsulant, in the solder bumps, and in the anisotropic film or adhesion interface. Samples observed with large void contents tended to correspond to those having higher thermal resistances. A means of sinking the heat generated by the active circuit should also be considered early in the product design phase particularly in handheld portable products. In isolated still air environments such as portable products, the heat generated by the ICs needs to be dissipated to the environment. The limited convection occurring off the back of the die and the substrate promote relatively high thermal resistances. Alternate approaches must be considered for even moderate power devices. Finally, assembly specifications for the DCA technologies should include detailed assembly procedures in order to minimize variability in the thermal dissipation characteristics from assembly to assembly. Such specifications should include adhesive/solder dispensing technique, dispensed amount, standoff tolerance, and maximum allowable void content.

Comparison of Experimental and Predicted Values

Average junction-to-ambient thermal resistance values for the unencapsulated flip-chip and encapsulated COB test vehicles are presented in Table 2. In general, the chip scale thermal model predicts $R_{\theta ja}$ for the solder attach and isotropic adhesive attach systems at 1 W with reasonable accurately. For the solder attach system, the error of the model prediction is 3 %; for the isotropic adhesive system, the error is 11 %. At the lower power range (0.1 W), the model losses accuracy in predicting $R_{\theta ja}$ with errors of 17 % and 16 % for the solder and isotropic adhesive samples, respectively. For the anisotropic adhesive attach, the model prediction error is 22% at 1 W and 39% at 0.1 W. With the exception of the anisotripic adhesive interconnect, the chip scale thermal model is found to estimate the junction to ambient thermal resistance of the flip chip systems with reasonable accuracy. For the anisotropic adhesive, the model accuracy is limited due in part to the lack of thermal property knowledge for these advanced interconnect materials.

Tables 3 through 5 present a comparison of the experimental and predicted temperature profiles for the DCA thermal management test vehicles at two power dissipation levels. Table 3 presents the results for the solder attach samples, Table 4 for the isotropic adhesive attach samples, and Table 5 for the anisotropic adhesive attach samples. In general, the chip scale thermal model predicts the junction temperature and the chip surface temperature within an accuracy of 1 to 13 %. The model's predictive capabilities for the board and substrate temperatures are typically less having prediction accuracy ranging from 1 to 18 %. These results are quite encouraging indicating that the chip scale thermal model, as verified by the experimental results presented, provides a relatively accurate means of estimating thermal dissipation in flip chip on board or direct chip attach assembly configurations. The results also indicate the importance of accurate material property data for the interconnect system. Moreover, the chip scale thermal model provides for a convenient design tool that can provide useful thermal dissipation data early in the design process allowing for "what if" scenarios to be run.

The results for the anisotropic adhesive attach test vehicles (Table 5) show a considerably less accurate prediction of the temperature profile. This is attributed to the lack of available thermal conductivity data for these materials. The thermal conductivity used was based on a rule of mixtures approximation for an epoxy adhesive filled with a known percentage of hollow metallized conductive spheres. The size, distribution, and concentration of the conductive spheres

[1] Based on a 228 mil square die, 32 mil FR4 substrate, 1 ounce Cu/Ni/Au traces, 25 °C ambient temperature, and a maximum junction temperature of 125 °C.

was determined from microscopy analysis of test vehicle cross-sections. Cross-section analysis was also used to determine the geometric parameters of Figure 6. Independent analysis was performed to determine the attach thermal conductivity comprised of the anisotropic adhesive compressed between the bump and trace (see Figure 6) and the underfill thermal conductivity comprised of the uncompressed anisotropic film.

The chip scale thermal design model is also useful in identifying the primary thermal dissipation paths for the various DCA technologies. The results are given in Table 6. In all cases, the smallest thermal resistance was found to be through the interconnects consisting of the bump, the attach, and the traces. This was typically a factor of 3 lower than the substrate path consisting of the convection off the back of the substrate and the fin heat transfer effect of the substrate. It is clear then that the primary thermal dissipation path for the flip chip systems studied is through the interconnect system and circuit traces. This suggests that an effective thermal dissipation technique would be the addition of thermal vias, power planes, and ground planes in flip chip substrate designs. This would tend to increase the effective heat transfer are of the interconnect and trace system thereby lowering the effective junction to ambient thermal resistance.

Overall, the predictions of the chip scale thermal design model show reasonably accurate agreement with the experimental results verifying the applicability of the model for three general DCA interconnect systems. The focus of future efforts will be in improving model accuracy and improving the repeatability of experimental measurements. In particular, secondary heat transfer paths will be investigated and more accurate materials properties will be incorporated. To reduce variability in the experimental measurements, the test vehicle assembly process will be improved to minimize void formation in the interconnects and underfill. Finally, the influence of process defects on thermal performance will be studied.

Conclusions

An experimental characterization of three DCA interconnect technologies has indicated a clear thermal performance difference between the technologies relative to baseline thermal performance data for chip on board test vehicles. The highest thermal performance interconnect system was the anisotropic conductive adhesive having up to a 42 % lower junction-to-ambient thermal resistance compared with the encapsulated COB assemblies. The isotropic conductive adhesive showed the next lowest $R_{\theta ja}$ up to 24 % lower than the encapsulated COB assemblies, and the solder attach assemblies showed the next lowest $R_{\theta ja}$ up to 8 % lower than the encapsulated COB assemblies. The junction-to-ambient thermal resistances were also found to decrease with increasing power, indicating that somewhat higher power densities can be achieved as the system power is increased. It was also found that glob top encapsulants provide additional heat spreading thereby lowering thermal resistances. In addition, a series of preliminary DCA thermal management design guidelines were presented.

A chip scale thermal design model has been developed for DCA assemblies and has been verified based on three DCA assembly technologies. Model predictions for junction-to-ambient thermal resistance and temperature profiles within the assemblies were found in good agreement with experimental measurements for solder attach, isotropic adhesive attach, and anisotropic adhesive attach systems. For the solder attach system, the average chip junction temperature and chip surface temperature were predicted within 1 and 2 %, respectively. In all cases, the primary thermal dissipation path was through the interconnect system comprised of the chip bump, attach material, and substrate trace. For the solder attach assemblies this path was 103 °C/W compared to 344 °C/W and 4311 °C/W for the other paths. Therefore, to improve the passive thermal performance of DCA assemblies, emphasis should be placed on reducing the thermal resistance of the interconnect system. This can be done by incorporating thermal vias, power planes, ground planes, and signal planes in multi-layer substrates.

Acknowledgments

The authors would like to thank the Georgia Institute of Technology's Manufacturing Research Center (Project EM 96-029) and Packaging Research Center (NSF Engineering Research Center Contract # EEC-9402723) for supporting this research. The authors would also like to extend their gratitude to Mr. R. A. Tarbox, Dr. S. R. Nagel, Dr. W. G. Roberts, Dr. R. Armington, Mr. P. Shimkus, Ms. M. Regan, Dr. J. Fulton, Ms. P. Crawford, Ms. M. Schmit, Dr. R. Deshmukh, and Ms. L. King of Lucent Technologies Bell Laboratories Engineering Research Center for supporting this work and enabling much of the infrastructure necessary for the experimental work. Additional thanks goes to Drs. K. Azar and J. Segelken for their insightful comments on thermal resistance characterization of electronic packages.

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