Reliability Assessment of Flip Chip on Organic Board Using Power Cycling Techniques

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Abstract

During the reliability assessment of a flip chip on board assembly (FCOB) by environmental stress tests, the physical characteristics of the field operating conditions are not sufficiently addressed. The failure mechanisms active at the environmental stress test conditions may not be dominant at the service operating conditions. The magnitude and intensity of thermomechanical stresses experienced by a FCOB at service conditions are different from those in the environmental stress tests, which result in discrepancies between dominant failure modes in the field operating conditions and accelerated life test conditions. Driven by the non-field failure modes, design modifications and process improvements during the prototyping stage may be misled. A "service field-oriented reliability assessment" methodology is introduced in this paper to address this issue by using a power cycling technique. The associated experimental power cycling system for FCOBs field reliability assessment is developed in this research. The test vehicles are assembled using fine pitch flip chips and high-density interconnect (HDI) substrates. The in-situ continuities of individual Kelvin solder bumps and daisy chains of the FCOB assemblies are investigated during the power cycling tests. The physical failure modes are revealed by acoustic microscopy, cross sectioning and scanning electron microscopy. "Design for field reliability" is then achievable by the effective design modifications and manufacturing process improvements at the prototyping stage.

I. Introduction

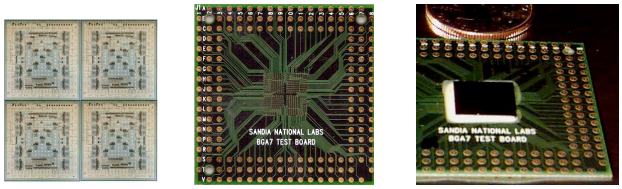
Flip chip on organic board assembly (FCOB) is an advanced electronic packaging technique developed to address the increasing need for miniaturization, low cost and high performance of an electronic system. The field reliability assessment of a FCOB assembly is critical for product design, manufacturing process development and supply chain management. During the product development stage, the field reliability performance information is not available to the designers and manufacturing engineers. Temperature thermal cycling and thermal shock tests are two environmental stress tests (ESTs) commonly used to assess the thermomechanical reliability of a flip chip assembly [1][2]. The validity of these tests is based on the assumption that the failure mechanisms active at the accelerated life test conditions are also dominant at the service operating conditions. However, the physical characteristics of service operating conditions are not sufficiently addressed by either thermal cycling or thermal shock tests. During a thermal cycling or a thermal shock test, the test vehicles are heated-up or cooled-down by an isothermal medium. The heat transfer occurs on the entire external surface of a test vehicle evenly. While for many powered FCOB assemblies, the main field thermomechanical stresses come from the internal local heating generated by the components' power dissipation, power on and off, mini-cycles during operation, and ambient temperature variation, etc. The magnitude and intensity of thermomechanical stresses experienced by the constituents of a FCOB at service conditions are different from those at a thermal cycling or thermal shock test. As a result, the failure modes exposed during the thermal cycling or thermal shock tests may not be the dominant ones at the service operating conditions. As a result, design modifications and process improvements at the prototyping stage are misled by the non-field reliability assessment obtained from these environmental stress tests. The discrepancies between the extrapolated lifetime of a FCOB assembly by a thermal cycling or thermal shock test and the actual service life will be significant. The field reliability performance of a FCOB assembly is a "black box" to the designers and manufacturing engineers. To track the field failure information is very time-consuming due to the relatively long service life of a product.

A "service field-oriented reliability assessment" method is introduced in this paper to address this issue. This method mimics the approximate field operating conditions on a product by using the power cycling technique. The physical characteristics of the power cycling better simulate the service operating conditions so that the power cycling is able to activate the field failure mechanisms and precipitate the field failure modes better than the thermal cycling and thermal shock tests. Previous investigations on CBGA and PBGA reliability using the power cycling technique show that power cycling can precipitate relevant field failure modes [3][4]. In this paper, a power cycling system is developed for the reliability assessment of a fine pitch flip chip on organic board assembly. This power cycling system is able to investigate the FCOBs reliability under different operating conditions. The reliability of the FCOB test vehicles assembled by capillary flow is investigated under a specific power cycling condition in this research. The in-situ electrical continuities of individual Kelvin solder bumps and daisy chains inside the FCOB assemblies are measured during the power cycling tests. The physical failure modes are revealed by acoustic microscopy, cross sectioning, and scanning electron microscopy. A linkage among the design, manufacturing process and the ultimate field reliability is established prior to the mass production. "Design for field reliability" is then achievable by the effective design modifications and manufacturing process improvements at the prototyping stage.

II. Test Vehicles

The ATC4.1 flip chips are used in this research (Figure 1). The chip is 456×456 mils in overall size with 1764 eutectic solder bumps in an area array format. The diameter of an eutectic solder bump is 5 mils. The bumps are at a 10 mils pitch. Daisy chains and Kelvin bump structures are built inside the chip for assessment of the interconnect reliability. Internal polysilicon heaters of a chip can heat the chip to the desired temperature to mimic the field operating conditions.

The substrate used for assembly is a low-cost and high-density interconnect (HDI) board with four layers of organic laminates. The overall size of the substrate is 1800×1800 mils. The pitch between the fine lines is 2 mils. The diameter of the flip chip pad is 3 mils. The diameter of the second-level probe pad is 100 mils. These probe pads are aligned along the periphery which are accessible by the spring probes. The test chip, HDI substrate and final FCOB assembly is shown in Figure 2.



(a) (b) (c)

Figure 1. Flip chip, organic HDI substrate and FCOB

The test chips are assembled onto organic substrates with dip-fluxing. The interconnects between chip and substrate are formed after the reflow process with eutectic solder profile. After the capillary flow underfill process, the FCOB assemblies are cured under the recommended temperature. The properties of the underfill used in this research are listed in Table 1.

Table 1. Underfill properties

CTE (ppm/^{0}C)	Tg (^{0}C)	Curing (^{0}C)	Modulus (GPa)
45	140	165	5.6

III. Power Cycling System Development

A power cycling system for the FCOB reliability assessment is developed in this research. The power cycling system contains a FCOB powering and cooling module, an in-situ interconnect continuity measurement module, a temperature sensoring module and a switch module (Figure 2). The terminals of daisy chains, Kelvin bump structures and heaters are wired out from the chip to the high-speed switch through a wiring interface. A four-point configuration is used to measure the resistances of the Kelvin bump structures. This eliminates the resistance measurement noises introduced by the external wires, copper traces and contact resistances. Thermocouples are attached on the die surface and substrate surface to monitor the real-time temperatures. The thermocouple wires are linked to a signal conditioner which sends the conditioned signals to an A/D card inside the controller.

Under the Labview software platform, the controller communicates with each discrete piece of equipment via the IEEE-GPIB interface. Associated application software is developed for the power cycling test in this research. For each test cycle, the activation of the continuity measurement is automatically controlled by the in-situ temperature sensoring. In the power-up cycle, the heaters are switched on to power the chip to the desired temperature. Once the chip temperature reaches the preset value, the controller activates the data acquisition sequence in the program. The resistances of individual Kelvin bumps and daisy chains are measured and stored in a data file by the controller. In the power-down cycle, the controller switches off the power and the cooling fan cools the FCOB assembly to the preset temperature. The resistances of individual Kelvin bumps and daisy chains at the high temperature and the low temperature are obtained.

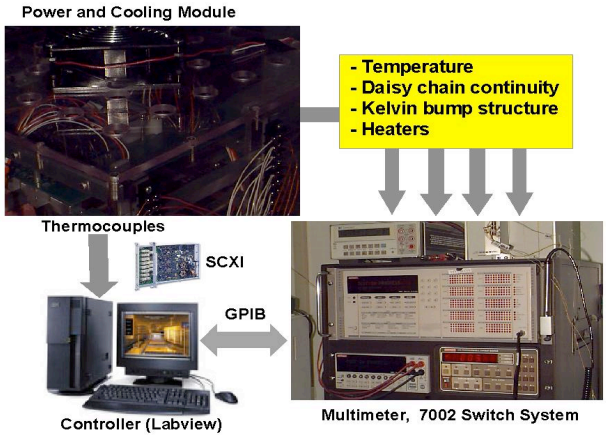


Figure 2. Power cycling test system

IV. Power Cycling Test Condition

Under the field operating conditions, the FCOB temperature increases very fast after switching on the power. The transient temperature gradients on the silicon and substrate are significant. When the heat dissipation steady state is reached, a temperature gradient through the FCOB thickness still exits. A power cycling profile is designed in this research based on the typical characteristics of the field operating conditions of powered FCOBs. The power cycling profile for the FCOB assembly measured by thermocouples is shown in Figure 3.

The power cycling temperature range is from 110^{0}C to 25^{0}C (room temperature). During the power-up cycle, the temperature gradients for silicon and organic substrate are very steep within the first 60 seconds. The maximum temperature gradients for silicon and substrate are about 1.6^{0}C/sec and 1.0^{0}C/sec, respectively. As the heat dissipation approaches the steady state, the temperature gradients drop dramatically. The temperature difference between the silicon and substrate is about 35^{0}C at the steady state. For the power-down cycle, the maximum temperature gradients are 1.2^{0}C/sec (for silicon) and 0.6^{0}C/sec (for substrate). The duration of one power cycle is about 5.8 mins.

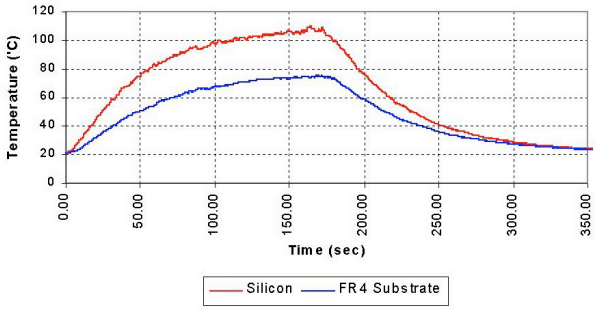


Figure 3. Power cycling thermal profile

V. Electrical Continuity of Solder Bumps

During the power cycling tests, the in-situ continuities of individual Kelvin solder bumps are monitored continuously by the four-point resistance measurement. The resistance measured within a Kelvin bump structure is the total resistance of UBM, collapsed solder bump and copper pad in the substrate. The UBM and copper pad are much thinner than the solder bump. The resistivities of the UBM and copper are relatively smaller than the resistivity of eutectic solder. Thus the resistance of the solder bump is dominant. The resistance change measured by the four-point configuration is a good indicator of the electrical continuity performance of a solder bump under the power cycling condition.

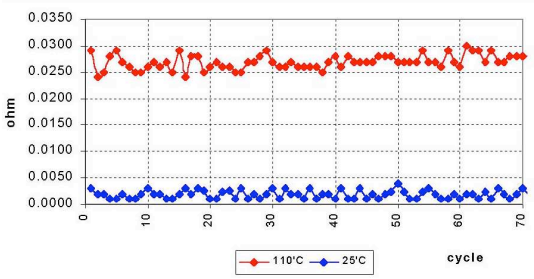


Figure 4. Single bump resistance during power cycling

As observed in the experiment, the resistance of a Kelvin solder bump changes cyclically during the power-up and power-down cycles. The measured resistances are within the range of 0.025~0.030 ohm at high temperature (110^0C) and 0.002~0.004 ohm at low temperature (25^0C) as shown in Figure 4. The locations of the solder bumps under investigation are located at the peripheral rows / columns of the ball grid array. The bump resistances measured at room temperature can well match the theoretical values calculated by the associated dimensions and material properties. For the resistances measured at high temperature, there is a significant discrepancy between the calculated resistances and the measured resistances. Given the temperature coefficient of resistance of eutectic solder, the resistance of a bump at 110^0C should be only 30% to 40% higher than its resistance at room temperature.

As the power cycling test continues, the solder bumps gradually degrade due to the thermal fatigue and crack propagation. The evolution characteristics of a bump continuity are investigated by in-situ monitoring of its resistance change. Two typical patterns of bump resistance change with respect to time are found during the power cycling test.

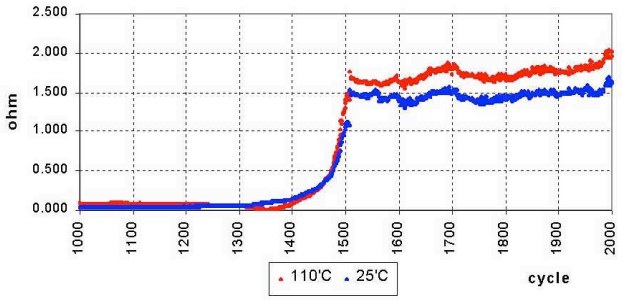


Figure 5. Bump resistance growth

One pattern is “gradual resistance growth – stabilization – intermittent failure – permanent failure”. After one to two thousand cycles, the resistances of a bump at both high temperature and low temperature gradually increase with time. There is no resistance spike during this resistance growth period. The resistances stabilize at a certain level for a period of time (Figure 5). Then intermittent failures start to occur. In most cases, the intermittent resistance failures occur at high temperature while the bump electrical continuity at low temperature is well maintained. With the further development of the crack interfaces, the intermittent resistance failures become permanent failures (open circuit) at high temperature. Meanwhile, the correspondent low temperature resistances are either at the stabilization level or at the “intermittent failure” phase (Figure 6). Among all the tests, there is no case in which a bump loses its electrical continuity at low temperature while well maintaining it electrical continuity at high temperature.

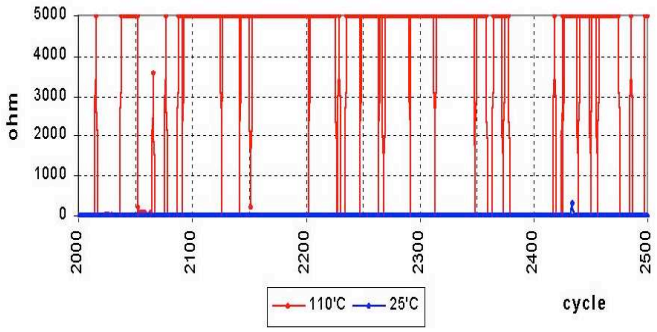


Figure 6. Bump intermittent failures at high temperature

Another pattern observed is similar to the first pattern except that there is no obvious “gradual resistance growth” phase. Instead, the resistance values jump promptly from the normal range directly to ×100 ohms. The spikes occur intermittently at the early stage. Then the resistances stabilize at this level for some time as shown in Figure 7. When the permanent failures occur at high temperature, the resistances at low temperature maintain at the ×100 ohms level for quite some time before jumping to the ×1000 ohms level (open circuit) as shown in Figure 8.

At the early stage of a power cycling test, the resistances at high temperature are always larger than those at low temperature due to the positive temperature coefficients of resistance of UBM, eutectic solder and copper.

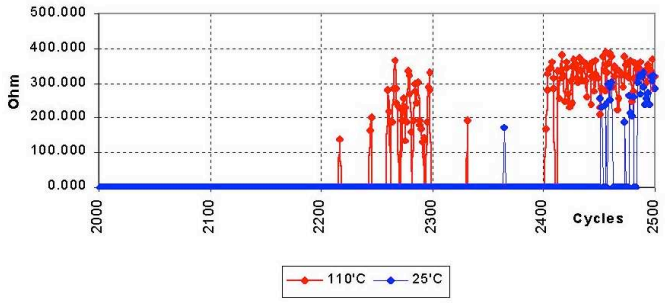


Figure 7. Intermittent resistance spikes

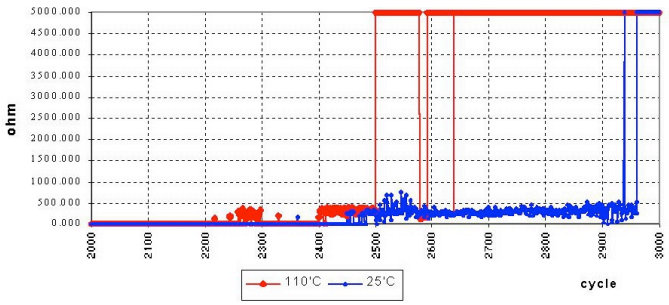


Figure 8. Permanent failure of a solder bump

The phenomenon of the electrical continuity loss only at high temperature is likely due to two reasons. One is the mismatch of Z-directional (through thickness) expansion between solder bumps and underfill material. Another is the convex bending (seen from the silicon side) of the substrate at high temperature. The CTE of the underfill used in this research is larger than that of the solder bumps. With the same temperature increase, the bumps are stretched vertically (in Z-direction) by the surrounding underfill. The top side temperature of the substrate is higher than that of the bottom side due to the heat diffusion. The positive temperature gradient through the substrate thickness results in the convex bending of the substrate. When there is a crack (either partial crack or complete crack) in the bump, during the power-up cycle, the Z-directional expansion of underfill and convex bending of the substrate physically enlarge the gap between the two cracked surfaces. Besides the impact of shear stresses on bumps caused by global CTE mismatch between silicon and substrate, the Z-directional expansion of underfill and convex bending of the substrate also accelerate the bump crack development in the horizontal direction. During the power-down cycle, the underfill around the bumps contracts and there is no more convex bending on the substrate. The two crack surfaces in a bump are pulled closer, which results in partially or completely recovering of the electrical continuity as shown in Figure 6 and 8. The duration of "resistance growth" is governed by the initial conditions of a bump, the quality of the UBM-bump interface and bump-copper interface, severity of crack initiation and growth, etc., which results in different patterns of bump electrical continuity evolution. For a solder bump, once the resistance stabilization phase is reached, the complete loss of its electrical continuity may occur at any time, especially at high temperature. The functionality of the associated circuitry becomes unreliable from the commencement of the bump resistance growth phase.

The evolution characteristics of daisy chains' resistances are not the same as those of Kelvin bumps. A daisy chain contains very long and thin copper traces on the substrate and Al/Ti/Cu/Ni interconnects on the silicon die, whose resistances are overwhelming compared to the bumps' resistances. In the power cycling test, once the cracks are initiated in a bump, it takes about 200 cycles for its resistance to increase to 0.5 ohm. The resistance changes of a bump during the crack initiation and the early crack growth phase can be captured by the Kelvin measurement. But these resistance changes are too small to be detected by the daisy chain resistance measurement. Only when the bumps experience serious cracks, are the significant changes observed in the daisy chain resistance measurements (Figure 9). For a daisy chain whose normal resistance is 5 ohms, if the interconnect failure criterion is 10% increase of the normal resistance, then a crack in a bump are only detectable after about 200 cycles from the point of the crack initiation. For most daisy chains investigated in the experiments, the loss of electrical continuity at low temperature occurs far behind that at high temperature.

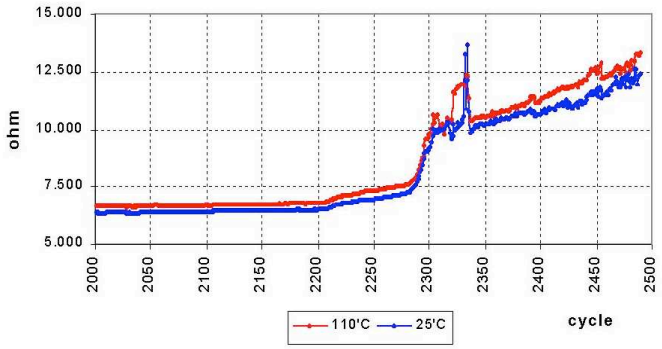


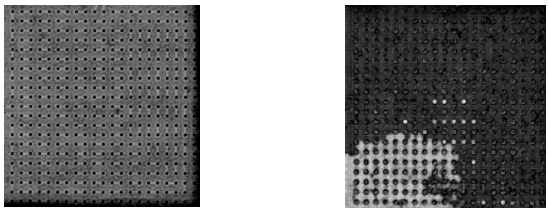
Figure 9. Daisy chain resistance characteristics

The characteristics of a bump continuity evolution are significant for the applications of thermal cycling and thermal shock tests for the FCOB reliability assessment. As seen from the experimental results, the loss of electrical continuity of a bump at low temperature occurs far behind that at high temperature. The off-line resistance measurement of a daisy chain or a bump at room temperature is not a sufficient criterion to determine the interconnects integrity. The crack initiation and early propagation in a bump are not detectable by either on-line or off-line resistance measurements of the associated daisy chain. The reliability assessment based on these daisy chain resistance measurements tends to be over-optimistic. The following-up statistical reliability analysis based on these daisy chain test results will result in significant discrepancies between the predicted lifetime and the actual service life of a product.

VI. Failure Mode Analysis

The failure modes exposed during the power cycling tests are analyzed by acoustic microscopy, cross sectioning and scanning electron microscopy.

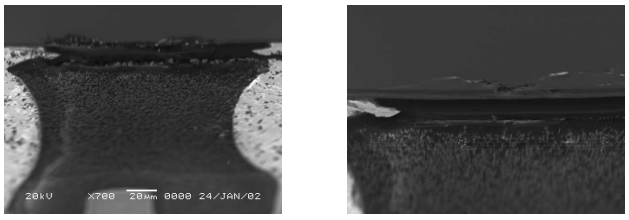
The interfaces within the FCOB test vehicles are investigated using acoustic microscopy (C-SAM). The test vehicles are periodically removed from the power cycling system and scanned off-line on the Sonoscan D-9000 after every 1000 cycles. Interface delaminations underneath the die are observed in some test vehicles after 1000 to 2000 cycles. Most delaminations are located at the corner area of the die. The C-SAM images of a FCOB before and after 1000 cycles are shown in Figure 10.



(a) (b)

Figure 10. Interface delamination underneath the die

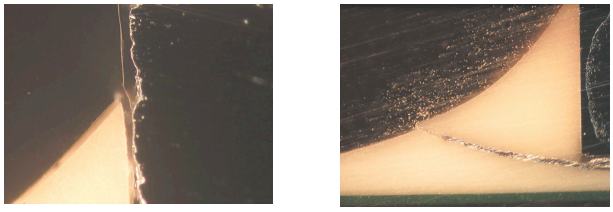
Further investigations on these delamination regions by scanning electron microscope reveal that the delaminations occur at the interfaces between underfill and passivation layer (Figure 11). The delaminations span the entire pitch between two adjacent bumps and stop at the UBM corners. The underfill-substrate (solder mask) interfaces demonstrate more robust thermomechanical reliability than the passivation-underfill interfaces. This is caused by the different inherent bonding properties of the underfill-substrate (solder mask) interface and passivation-underfill interface, as well as the different thermal excursion at each of these interfaces. As the silicon die serves as a heat source during the power cycling test, the temperature at the passivation-underfill interface is higher than that at the underfill-substrate interface. In the power-up cycle, the temperature of the silicon is about 110^0C, while the temperature of the substrate is less than 80^0C. The CTE difference between silicon and underfill is larger than that of underfill-substrate. The horizontal shear force at the passivation-underfill interface is larger than that at the underfill-substrate interface. Additionally, the convex bending of the entire underfill-substrate laminate due to the Z-directional temperature gradient also helps to segregate the underfill from the rigid passivation layer.



(a) (b)

Figure 11. Delamination at passivation-underfill interface

Besides the delamination of underfill underneath the die area, underfill fillet delaminations are observed as shown in Figure 12a. Horizontal fillet cracks are also observed, which extend into the underfill layer underneath the die (Figure 12b). One side of the underfill fillet tip is the silicon (heat source), another side is the convection air with low temperature. Under this thermal excursion, the fillet underfill near the silicon side surface tends to expand more than the die in the Z-direction. The fillet underfill exposed to ambient air contracts faster than the underfill near the die side surface. This tends to peel off the fillet from the silicon side surface.

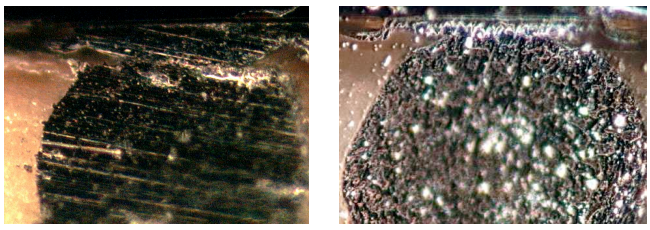


(a) (b)

Figure 12. Underfill fillet delamination and crack

Most interconnect cracks are found in the solder bumps near the UBM-bump interfaces (Figure 13). The bump-copper interfaces appear to be more robust than the UBM-bump interfaces during the power cycling tests. The global CTE mismatch between the silicon and substrate, the local CTE mismatch at UBM-bump interface and at bump-copper interface, the Z-directional thermal gradient are among the important influencing factors. The convex bending of the substrate during power-up cycle helps to initiate the cracks in bump corners. Once the delaminations at the passivation-underfill interfaces occur, the passivation layer no longer constrains the thermal expansion of the underfill. The underfill directly shears the bumps near the UBM-bump interface. This is an analogy to reducing bump stand-off height in a FCOB assembly without underfill.

The characteristics of cracked Kelvin solder bumps obtained from cross sectioning are correlated to their in-situ electrical continuity performance as shown in Figure 5 and 6. From the cross sectioning images in Figure 13, the crack interfaces in a bump, which are located right below the UBM-bump interface, can partially contact with each other at some portions at low temperature. The corrugated contact surfaces are not firm or stable. When the chip is powered, the upper crack surface and lower crack surface will be pushed away from each other by the combination of Z-directional expansion of underfill and the convex bending of the substrate. This results in complete loss of electrical continuity at high temperature.

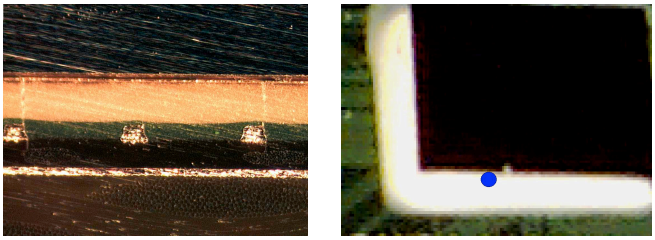


(a) (b)

Figure 13. Solder bump crack near UBM-bump interface

Another failure mode found during the power cycling tests is the vertical underfill cracks along the die edges. The

locations of these vertical cracks are randomly distributed along the silicon die edges. It is noticeable that almost every vertical crack is ended at one edge of a copper trace on the substrate as shown in Figure 14. These cracks extend to the top of the underfill layer underneath the die area. The stress concentration at the sharp corners of the copper trace is one of the major causes.



(a) (b)

Figure 14. Vertical underfill cracks and their locations

VII. Conclusions

The reliability of the flip chip on organic board assemblies is studied in this paper. The reliability of individual Kelvin solder interconnects is investigated by in-situ monitoring of their electrical continuities throughout the power cycling test. The resistances of a single bump in the Kelvin structure are quantitatively characterized at high temperature (110^0C) and low temperature (25^0C). Two typical patterns of bump continuity evolution are found in the experiments. One is "gradual resistance growth – stabilization – intermittent failure – permanent failure" and another one is "intermittent spikes – stabilization – intermittent failure – permanent failure". The loss of electrical continuity of a bump at low temperature occurs far behind that at the high temperature. The off-line resistance measurement of a daisy chain or a bump at room temperature is not a sufficient criterion to determine the interconnects integrity. The crack initiation and early propagation in a bump are not detectable by either on-line or off-line resistance measurements of the associated daisy chain. The failure modes observed during the power cycling test include cracks in solder bumps near the UBM-bump interfaces, horizontal underfill cracks at the under fillet region, randomly distributed vertical cracks in underfill, underfill delaminations at the fillet tip and underfill delaminations underneath the die area. Most underfill delaminations occur at the passivation-underfill interface.

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References

1. M. Pecht, Handbook of Electronic Package Design, Marcel Dekker, Inc., New York, 1991, pp.477-528
2. G. W. Xian, et al, "Reliability Study and Failure Analysis of Fine Pitch Solder Bumped Flip Chip on Low-Cost Printed Circuit Board Substrate", Proc 51 Electronic Components and Technology Conference, 2001, pp.598-605.
3. G. DiGiacomo, "Thermal Diffusion Model Describing Transient Strain in Chip Solder Joints During Thermal Cycling", Proc ISHM'92, 1992, pp.637-642.
4. Q. Qi, "Reliability Studies of Two Flip Chip BGA Packages Using Power Cycling Test", Microelectronics Reliability, Vol.41, 2001, pp.553-662.