FLUX-UNDERFILL COMPATIBILITY AND FAILURE MODE ANALYSIS IN HIGH YIELD FLIP CHIP PROCESSING

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Abstract

The compatibility of flux and underfill material systems significantly contributes to the formation and growth of process-induced defects and further influences flip chip reliability. Various no-clean fluxes, along with a water-soluble flux used as the baseline, are tested with two fast flow, snap cure underfills. Liquid-to-liquid thermal shock and temperature and humidity tests are conducted to evaluate the reliability of each flux-underfill material system.

The failure modes, specifically underfill delamination, solder fatigue, and die cracking, are identified and analyzed. The correlation among process manufacturing defects, failure modes, and long-term reliability are determined. Understanding these failure modes will further enable and facilitate the implementation of low cost, high yield flip chip processing in standard surface mount technology.

Introduction

There are numerous factors, such as chip and board design variables, process parameters, material selection, and throughput issues, that govern flip chip process yield. Fluxing, chip placement, reflow, underfill dispense, and underfill cure are the processes of flip chip assembly illustrated in Figure 1. Of the many challenges in flip chip processing, the compatibility of flux and underfill merits special consideration in order to provide a robust flip chip process window and acceptable reliability. This issue has to be studied to investigate the effects on yield and failure modes. It is critical to identify and discuss the failure modes to understand how flip chip devices fail in order to characterize the feasibility of flip chip processing using a no-clean flux system.

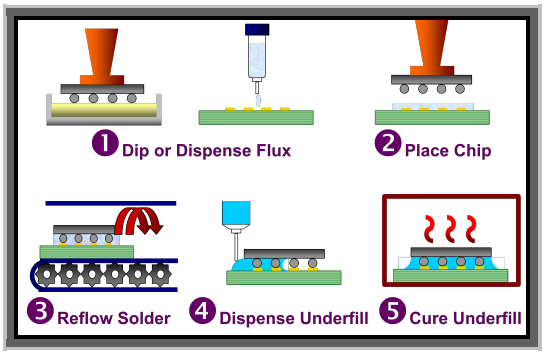

Figure 1 Low cost flip chip process flow.

Experimental Methodology

Description of Test Vehicles

The substrates used for the reliability testing are FA10 2x2 FR-4 substrates that are 0.79 mm (31 mil) thick, and 14.6 cm x 7.6 cm (5.75 in x 3 in) in dimension. The bond pad metallization is Cu/Ni/Au. There are 10 bond sites per substrate. The test chips, provided by Flip Chip Technologies, are eutectic Sn/Pb solder, full area array with 317 I/Os, daisy-chained chips that are 5.08 mm x 5.08 mm (0.2 in x 0.2 in) in size. The chips have a silicon nitride passivation layer and a UBM of Al/NiV/Cu.

Procedures

Six no-clean fluxes along with a water-soluble flux have been tested to evaluate their performance by comparing with a control water-soluble flux [1]. The no-clean fluxes are labeled Fluxes A-F, while the water-soluble flux is named the Control Flux. Fluxes A, B, C and the Control Flux are dispense fluxes; and Fluxes D, E, F are dip fluxes. The three criteria to evaluate the fluxes are quadrant yield

percentage via electrical continuity testing, interconnect voiding percentage, and interconnect shear strength via die shearing. Electrical continuity testing is based on chip, column, and interconnect yields. The solder voids are detected under X-ray microscopy to observe the number and size of voids before chip placement and after reflow. The shear test distinguishes the fluxes by the shear strength such that a higher shear force tends to indicate better adhesion and more robust interconnects [1].

The flux evaluation, based on an Archimedean ranking technique, determines that Fluxes A, D, F, and the Control Flux perform better and are utilized for assemblies implementing two different fast flow, snap cure underfills (labeled Underfills A and B). These assemblies are placed in liquid-to-liquid thermal shock (LLTS) testing and temperature and humidity (T/H) testing to assess their reliability with respect to eight different flux-underfill material system combinations [1].

Table 1 Underfill material properties.

Property	*Underfill A*	*Underfill B*
CTE (ppm/°C)	35	28
Filler Content (%)	40	62
Viscosity (cP)	8,000	10,000
Tg (C)	130	144

The underfills, described in Table 1, are selected because of their distinctive difference in material properties and flow characteristics. Underfill A has a higher CTE and a lower filler content whereas Underfill B has a lower CTE and a higher filler content.

The experimental matrix is presented in Table 2. Thirty assemblies are built for each material system. An L-shape dispense pattern is employed for Underfill A samples; and a one pass, I-shape dispense pattern for Underfill B samples. For LLTS testing, the samples are subjected to two temperature baths of extreme temperatures (-55 and 125°C), whereas for T/H testing, the samples are tested under the conditions of 85°C and 85% relative humidity.
Electrical continuity of each daisy-chained loop is a means of determining failure. A chip whose resistance exceeds the threshold of ±10% of the original resistance at time zero before cycling is considered a failure. In addition, if a sample is detected with a die crack based on C-SAM analysis, it is also regarded as a failure, despite that the sample may still maintain electrical continuity.

Table 2 Experimental matrix.

Material Combinations		*Liquid-to-Liquid*	*Temperature/ Humidity*
Flux	***Underfill***	***Sample Size***	***Sample Size***
Control	***A***	30	30
Control	***B***	30	30
A	***A***	30	30
A	***B***	30	30
D	***A***	30	30
D	***B***	30	30
F	***A***	30	--
F	***B***	30	--
Total No. Of Samples		240	180
Testing Conditions		55C/125C	85C/85%RH
Continuity Check		Every 100 Cycles	Every 100 Hours
C-SAM		Every 200 Cycles	Every 200 Hours
Last Test		Until Failure	1000 Hours

LLTS Results and Analysis

Underfill A

Figure 2 presents the Weibull distribution plot of the LLTS failure rate of each flux sample with Underfill A. The results are summarized in Table 3. In general, the first failures of the Underfill A samples occur after only 200 cycles. Most of the early life failures are caused by die cracking, discussed below. Flux D demonstrates the best compatibility with Underfill A, with a mean time to failure of 1490 cycles, 264 cycles more than the Control samples. Flux F and Flux A excel in terms of solder wetting and yield [1], but they do not perform well in terms of reliability testing with Underfill A.

While most of the other samples fail due to electrical continuity loss, numerous test vehicles with Flux F exhibit a propensity for die cracking, with several samples cracking after 200 cycles. An additional Weibull distribution analysis is performed for Flux F samples excluding die cracking as a failure mode. It shows that if die cracking is neglected, Flux F samples generate a much higher reliability life of 1687 cycles. It also has a much larger Weibull shape parameter of 10.63, which describes the slope of the Weibull distribution and is related to the failure rate.

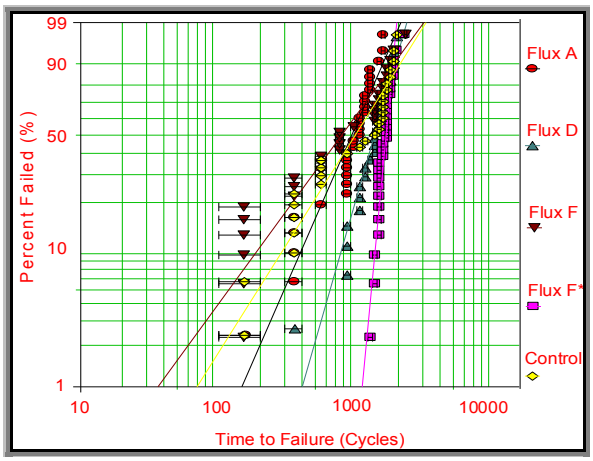

Figure 2 Weibull distribution for Underfill A.

Table 3 LLTS testing results for Underfill A

Flux	*Underfill*	*First Failure*	*Last Failure*	*Weibull Life*	*Shape Parameter*
Control	A	200	2000	1226	1.60
A	A	200	1600	1076	2.31
D	A	400	2000	1490	3.51
F	A	200	2300	1003	1.38
F*	A	1300	2300	1687	10.63

** denotes results excluding die cracking as a failure mode.*

Underfill B

The results for each flux sample with Underfill B are summarized in Figure 3 and Table 4. Figure 3 presents the Weibull distribution plot that depicts the LLTS failure rate of each material system.

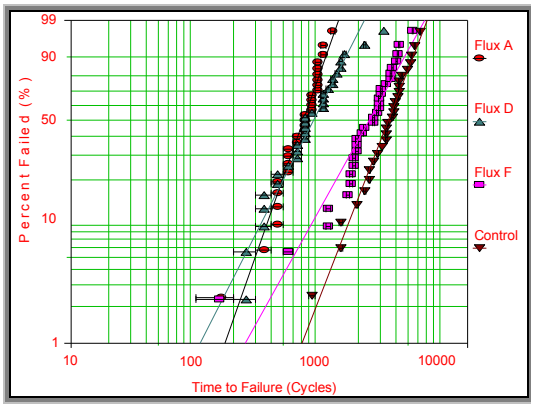

Figure 3 Weibull distribution for Underfill B.

Table 4 LLTS testing results for Underfill B

Flux	*Underfill*	*First Failure*	*Last Failure*	*Weibull Life*	*Shape Parameter*
Control	B	900	6300	4006	2.65
A	B	200	1300	824	2.92
D	B	300	3200	1051	2.02
F	B	200	5500	2983	1.85

For Underfill B-Flux A samples, the mean time to failure is 824 cycles. It is apparent that this material combination is not particularly compatible in terms of reliability. On the other hand, Flux D, which is not compatible with Underfill A, performs well with Underfill B, having a Weibull life of 2983 cycles. The Control samples perform very well, with a Weibull life of 4006 cycles.

Flux-Underfill Compatibility

Comparing the results of these eight material systems, Underfill A works the best with Flux D, with a life of 1490 cycles. Underfill B is not particularly compatible with Fluxes A and D, but it is compatible with Flux F. Underfill B-Flux F samples provide the largest number of cycles for the no-clean process with a mean time to failure of 2983 cycles. Underfill B performs well with the water-soluble Control Flux, having a life of 4006 cycles; and with Flux F. This is an indication that Underfill B is capable of effectively reducing the CTE mismatch between the chip and the substrate. In fact, the Control Flux-Underfill B samples last 2780 cycles longer than the Control Flux-Underfill A samples.

Effects of Underfill Voiding

It is found from C-SAM images that there are some samples that contain underfill voids after cure. The formation of underfill voids is attributed predominantly to the dispense pattern, dispense parameters, insufficient underfill volume, and the flux residue remaining after reflow. The L-shape dispense pattern might instigate voids in the center of the chip where the two flow fronts meet and generate shadow voids or capture voids due to flow front instability (Figure 4).

Voids formed with the I-shape dispense pattern are generally seen near the edge opposite of the dispensed edge, shown in Figure 4. This type of void is generated because the underfill flows along the left and the right edges faster than through the solder joints in the center. The flow fronts converge near the lower center of the chip, entrapping air and creating capture voids. The justification of underfill void formation is confirmed by underfill flow characterization studies [2].

Another cause is flux residues. Because no cleaning procedure is employed with the no-clean flux samples, some flux residue can remain around the solder joints or along the edges of the chip. Such residue can block the underfill from flowing through the gaps between solder joints; thus voids can be generated randomly near solder joints. An example is shown in Figure 5 for Flux A in which residues are observed along the chip edges. This occurrence is flux specific and random regardless of the dispense pattern.

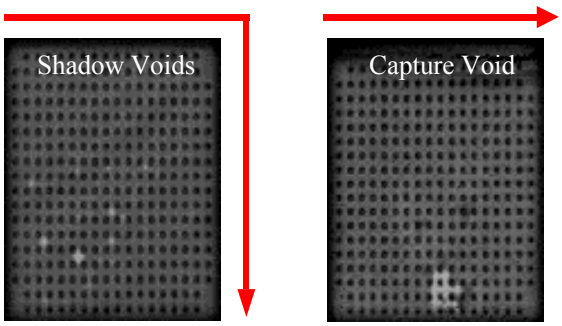

Figure 4 Underfill voids caused by dispense pattern.

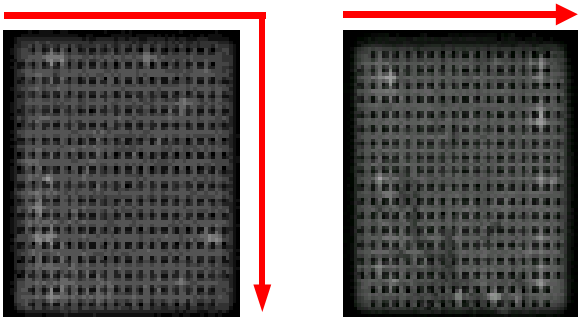

Figure 5 Underfill voids caused by flux residues.

In terms of the impact of underfill voiding on reliability, the effect is not strictly detrimental to the reliability data, since all Underfill A material systems and all but one of the Underfill B material system survive more than 1000 cycles. In general, samples with underfill voids do not exhibit a significant impact on reliability. In order to determine its effect, the Control samples are studied because they do not have flux residues that can reduce device reliability life.

Figure 6 presents the sequential C-SAM images of a Control Flux sample with Underfill B undergoing LLTS testing. This sample is selected because of its large underfill void, which is the worst case process defect caused by the I-shape dispense pattern. Small areas of underfill delamination start after 200 cycles, and they are scattered around the chip as the testing continues. The solder joints inside the void start to experience some weakening after 2000 cycles. Delamination is detected at the bottom right corner after 3500 cycles. It finally fails electrically after 4300 cycles at columns 1, 16, and 17, due to delamination and solder fatigue. Note that the region where the void is present retains electrical continuity despite the severe solder fatigue as illustrated by appearance of the white C-SAM signature of the joints in the voided location.

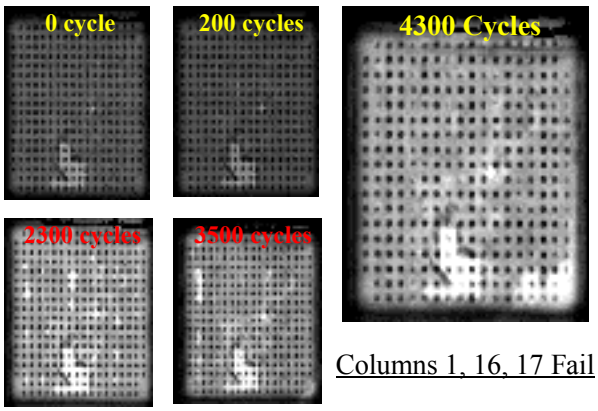

Figure 6 C-SAM images of a Control sample with a large underfill void.

Finite element analysis of flip chip assemblies during thermal cycling performed by Schubert, et al. [3] shows that the magnitude of the maximum accumulated creep strain on samples with a small underfill void near the center is equivalent to that of samples with no voids. Samples with a big void actually have lower creep strains because the overall stiffness of the assembly is decreased. However, voids can still generate stresses and strains because of the CTE mismatch. As such they can cause nearby solder joints to fail sooner because of rapid fatigue [3].

LLTS Failure Mode Analysis

The primary failure modes identified in the LLTS testing are underfill delamination, solder fatigue, and die cracking. The most prevalent failure is delamination at the chip passivation-underfill interface that eventually leads to solder fatigue failure. Figure 7 shows typical delamination detected in reliability testing: column or row delamination in the spacing between solder joints, bulk (massive) delamination, and delamination around corners or edges of the chip. There is also halo delamination, forming a ring-like shape around individual solder joints. Halo defects are typically caused due to the existence of flux residues around the solder, promoting local delamination.

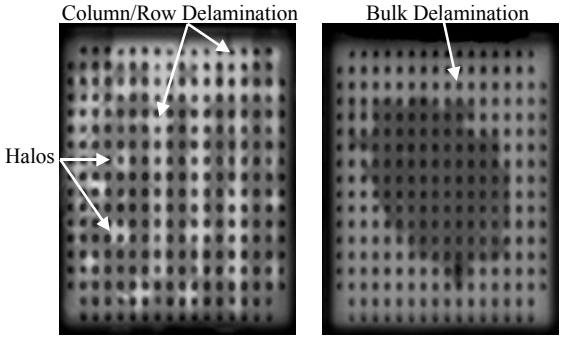

Figure 7 Examples of underfill delamination.

Solder fatigue cracks, shown in Figure 8, account for most of the electrical failures observed in LLTS testing. Underfill delamination generally leads to local solder fatigue failure in high stress regions as the testing progresses. When there is a crack in the solder, an elevated resistance reading or an open loop is found.

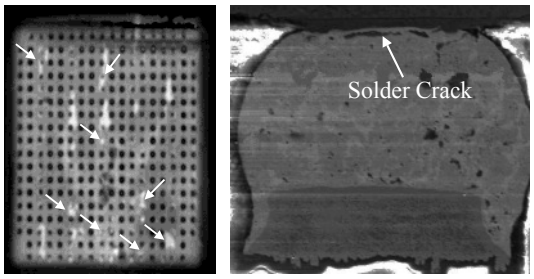

Figure 8 Solder fatigue cracking.

Die cracking is observed in some of the samples. It is detected via C-SAM images. It appears as a dark line running through or along the edges of a chip. Figure 9 presents three examples of die cracks located near the edge of the chip. Die cracks generally originate from the chip edge. They grow inside toward the solder joints due to the large stresses and stress risers along the edges of the chip caused by the global CTE mismatch between the chip and the substrate, bending effects at the chip edges, silicon die defect, and assembly warpage.

Table 5 presents the breakdown of failure modes of all the LLTS samples. Notice that delamination that leads to solder fatigue is the most prevalent failure mode in LLTS testing. For Underfill B samples, more than 60% of all samples fail due to delamination/solder fatigue.

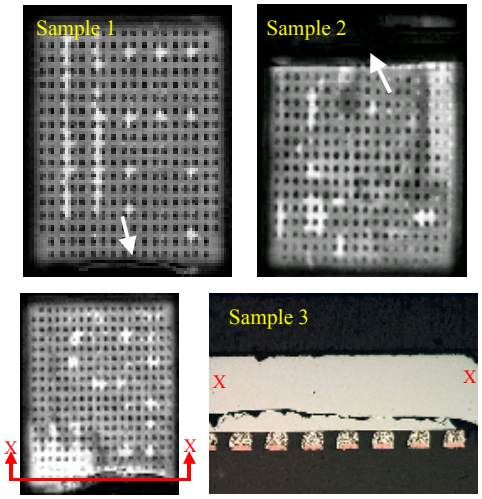

Figure 9 Examples of die cracking failures.

Table 5 LLTS failure modes.

Flux-Underfill	*Total Failure*	*Delamination/ Solder Fatigue*	*Die Cracking*
Underfill A			
A-A	100%	66%	34%
D-A	100%	79%	21%
F-A	100%	23%	77%
Control-A	100%	55%	45%
Overall	100%	56%	44%
Underfill B			
A-B	100%	100%	0%
D-B	100%	95%	5%
F-B	100%	72%	28%
Control-B	100%	63%	37%
Overall	100%	83%	17%

Figure 10 shows an example of delamination that starts from the chip-underfill interface, and penetrates towards the bulk underfill along the edge of the solder joint. This debonding of underfill is so severe that it actually propagates through the underfill layer and into the solder mask and substrate, causing substrate cracking.

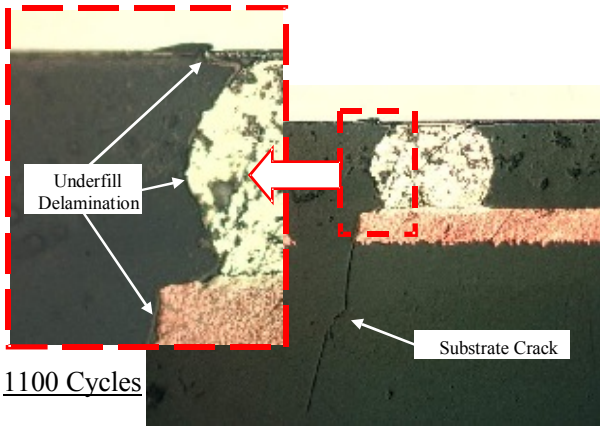

Figure 10 Underfill delamination and substrate cracking found in a Flux D-Underfill B sample.

For Underfill A samples, die cracking is a commonly detected failure mode that occurs as early as 200 cycles. For the Flux F samples, 77% of the samples fail due to die cracking. C-SAM and cross-section images of die cracking are shown in Figure 11. In this case, the crack originates from the corner of the chip where the crack is more defined. It propagates downward and into the bulk of the silicon until it encounters a uniformly distributed stress level and it starts to propagate parallel along that plane. This is an example of an in-plane crack that occurs over time that is believed to be static fatigue [4]. As the testing continues, the crack moves down to the chip passivation and eventually affects the device operation and solder joints. It is believed that such a crack is generally caused by silicon chip defects from wafer dicing in combination with large underfill stresses.

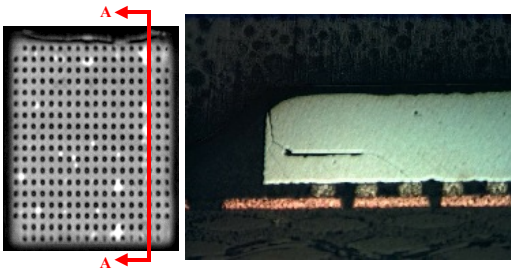

Figure 11 Die cracking found in a Flux D-Underfill A sample.

Occasionally, a die crack would occur abruptly after extensive thermomechanical stress exposure. Figure 12 illustrates the C-SAM images of a Flux F-Underfill A sample in which no die cracking is observed after 1400 cycles. But 100 cycles later, large cracks across the chip occur. A row cross-section (plane B-B) image of the cracks is also presented to depict the severity of this failure mode.

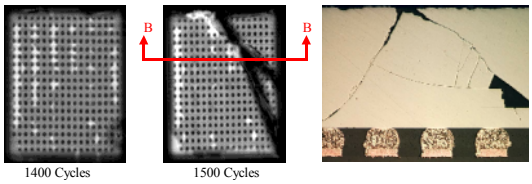

Figure 12 Die cracking found in a Flux F-Underfill A sample.

Underfill cracking is another failure mode observed. The underfill cracks are found after samples are cross-sectioned. This failure mode has not been documented in the past for fast flow, snap cure underfills. It is detected in both the bulk underfill material between solder joints (Figure 13) and in the underfill fillets (Figure 14). This failure mode is underfill specific because only Underfill A exhibits such phenomenon, but not Underfill B. A larger amount of filler concentration in underfill increases its strength and stiffness. Since Underfill A has a lower filler content with 40%, it tends to crack after undergoing thermal shock testing.

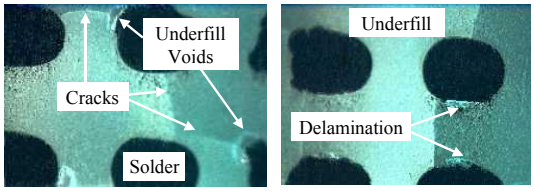

Figure 12 Bulk underfill cracking.

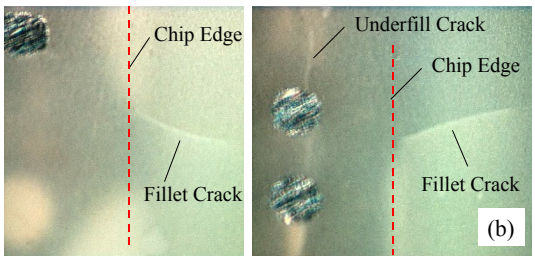

Figure 13 Bulk underfill cracking.

T/H Results and Analysis

The T/H testing results are summarized in Table 5. In general, Underfill A samples are more resistant to temperature and humidity exposure. Both Flux A and Flux D samples perform better than the Control samples for both underfills. The results for Underfill B indicate lower reliability performance than expected. Moreover, there is a clear indication of the incompatibility of Underfill B with the Flux D. This outcome demonstrates that evaluating additional no-clean fluxes is essential to effectively determine the compatibility of flux and underfill material systems.

Table 5 T/H results for Underfills A and B.

Flux	*Underfill*	*Passed 1000 Hours*	*Percent Passed*
Control	A	27/30	90%
A	A	27/29	93%
D	A	33/35	94%
Control	B	16/28	57%
A	B	25/28	89%
D	B	23/35	66%

The T/H test accelerates moisture absorption and penetration to flip chip packages through the underfill material. The moisture can deteriorate the adhesion of the underfill material to the passivation, solder, and solder mask; and thus delamination can be observed especially around the edges and corners of the chip, shown in Figure 14.

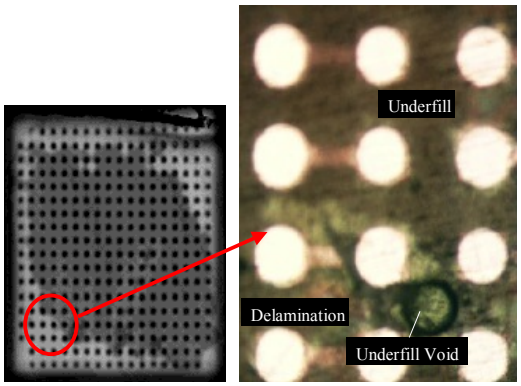

Figure 14 Underfill delamination seen in a Flux A-Underfill B T/H sample.

In some cases, it also penetrates into the UBM layer and compromises the adhesion of the UBM to the chip, causing the UBM pad to lift (Figure 15). Failure in T/H testing is typically a high resistance measurement driven from underfill delamination, UBM pad lift, and/or micro-cracks in the solder joints. It has been shown that the delamination around the edges can lead to large stress concentration near the solder interconnect that eventually fail due to thermomechanical stress.

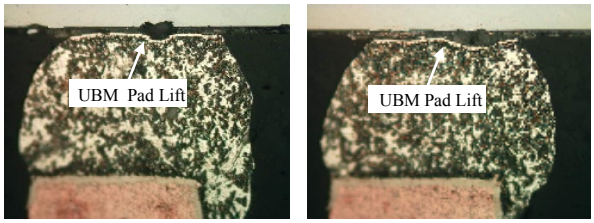

Figure 15 Examples of UBM pad lift failure.

Conclusions

Robust and repeatable process windows for no-clean fluxes have been established to assemble high yield flip chip packages. It is demonstrated that satisfactory reliability is attained with several material systems, with all but one LLTS material system passing a mean time to failure of 1000 thermal shock cycles. The thermal, mechanical, and electrical phenomena of flux-underfill compatibility greatly influence flip chip reliability. The demonstration of compatible flux-underfill material systems promotes the application of flip chip in surface mount assembly. The feasibility of implementing flip chip processing relies on such information and reliability data to characterize a specific process for microelectronic applications. Based on the results presented, robust flip chip process yield and satisfactory reliability can be achieved with a no-clean process for commercial applications.

References

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[4] Sylvester, M., et al., "Thermal Cycling Effects on Eutectic Flip-Chip Die on Organic Packages," *Proceedings of 2000 International Conference on High-Density Interconnect and Systems Packaging*, April 2000, pp.438-443.