Flip Chip Processing Using Wafer-Applied Underfills

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Abstract

Wafer-level underfill has the potential to substantially increase the implementation and usage of flip chip technology in the electronics industry. The development of wafer-level underfills can bring the financial benefits of wafer-level processing to flip chip assembly and packaging. In order to realize these benefits, the wafer-level flip chip process should be transparent to standard assembly lines.

Experimental studies have identified a number of process-related defects, including underfill voids, underfill outgassing, and die misalignment resulting from the solid to liquid transition of the wafer applied underfills and their associated surface tension. In the current study, aspects of assembly processing that relate to wafer-level flip chip assembly quality are examined. A parametric study of the effect of underfill coating uniformity on assembly quality and underfill voiding is presented. To address the surface tension driven die misalignment, a method is explored for reducing die misalignment through the use of fillet-constraining solder mask patterns. In addition, a theoretical description of the forces acting on a wafer-level flip chip die is developed to better understand the influence of process and design parameters on assembly yield.

Introduction

With the continued proliferation of low-cost, portable and high-functionality electronic devices, there is a high demand for electronic packaging that can be implemented profitably and reliably. Flip chip packaging technology is well suited to this market, as it is characterized by lower costs, shorter signal paths, and higher I/O densities than comparable wirebond interconnect packages. However, a concern with conventional flip chip packaging has been its throughput and underfill production issues. The amount of time required to dispense, flow, and cure the underfill can be an obstacle to adoption. Moreover, as device sizes increase and IO counts increase, conventional capillary flow underfills fail to meet the process and reliability requirements of high end packaging applications (e.g., ASICs and microprocessors). Vast improvements have been made in the flow times of capillary underfills, but the performance of these materials is reaching a plateau [1].

A proposed modification to the flip chip process is the application of underfill at the wafer level, eliminating the dispense, flow, and separate cure steps associated with assemblies utilizing capillary-flow underfills. In addition, the wafer-level material should include fluxing capabilities similar to no-flow underfills, in order to provide true transparence to assembly lines.

In this paper, some of the key issues facing the assembly of wafer-level flip chip die are addressed. In previous experimental builds, underfill voids have been observed. Such voids have a negative effect on both wafer-level interconnect yield and long-term reliability. The effect of underfill coating uniformity on wafer-level flip chip assembly quality, including voiding, is studied parametrically. In addition, experimental evidence has shown wafer-level flip chip assemblies frequently misalign during underfill liquification and die collapse. A method to constrain fillet wetting for the purpose of reducing die alignment is explored. Also, a theoretical description of the forces acting on wafer-level flip chip die during collapse is presented to clarify some of the physical phenomena that govern wafer-level flip chip assembly.

Background

The major steps required to manufacture a wafer-level package include application of the underfill film to a bumped wafer, dicing of the wafer (in some instances the latter two steps are reversed), and subsequent packing of the coated chips (see Figure 1). To attach the wafer-level package to a substrate, the assembler processes the package alongside standard SMT components, using a high-speed placement machine and a conventional reflow oven, as depicted in Figure 2. The fluxing capability of the wafer-level package is self-contained, and collapse and cure of the underfill package occur simultaneously with the reflow of the other components during a typical solder reflow profile. In developing the wafer-level flip chip assembly process, the reflow portion of the process has been troublesome to date, with numerous process defects occurring. The most significant process defects include underfill voiding and die misalignment during collapse.

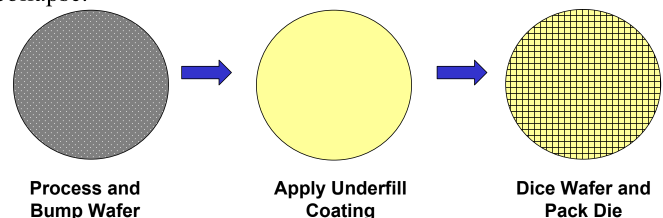

Figure 1. Wafer-level packaging process: fabrication.

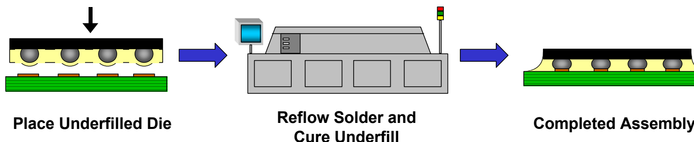

Figure 2. Wafer-level packaging process: board-level assembly.

Underfill voids are undesirable at any stage of the assembly process because they can compromise alignment prior to reflow, interfere with solder interconnect formation, and negatively affect the long-term reliability of the assembly. The presence of entrapped air in the underfill prior to coating may be problematic depending on the viscosity of the underfill and the quantity of entrapped air. Potentially, significant amounts of entrapped air in a thick, viscous underfill could remain in the underfill bulk for the duration of the assembly process, resulting in numerous small voids or a few large voids if the air bubbles collect together. To eliminate the problem of entrapped air in the underfill prior to coating, it is advisable to vacuum pack the material before applying to the wafer. Furthermore, underfill outgassing can occur during heating, typically as a result of the chemical reaction that occurs at flux activation or as a result of gaseous effluents in the polymer material. Adjustments can be made to the temperature profile to attempt to reduce the chemical outgassing, but severe outgassing generally requires material reformulation.

Experimental Plan

A parametric experiment is developed to study the effect of varying coating uniformity on the quality of wafer-level flip chip assemblies. This experiment examines the effects of initial coating roughness on the alignment and percentage of voids in wafer-level flip chip assemblies. A very rough coating surface is likely to lead to an increased percentage of voids in the final assembly, due to the entrapment of air during underfill liquification. Also, roughness can lead to uneven liquification of the underfill coating, asymmetric wetting, or non-level positioning of the chip, all of which may cause misalignment during the reflow process. Therefore, it is important to determine if underfill coating uniformity is a significant factor in wafer-level flip chip assembly. The flip chip test vehicle assemblies are evaluated by determining voiding and misalignment.

To ensure enough underfill is present to generate fillets upon liquification, many die require an underfill coating thicknesses that exceeds their bump height. In such a situation, the die rests on a mass of underfill that becomes liquidus at elevated temperature. The die must collapse through the underfill and come to rest on the substrate with the correct solder bump/substrate pad alignment. Die misalignment is a phenomena in which the wafer-level flip chip die is affected by an imbalance of horizontal forces during collapse largely driven by underfill surface tension, which results in a translation and/or rotation with respect to the substrate pads. The die misalignment phenomena is not constrained to cases where the underfill covers the bumps. In instances where the flip chip bumps are exposed beyond the underfill film, the liquefying underfills can cause mis-alignment overcoming the frictional forces between the bumps and substrate pads.

A designed experiment is developed to study the effect of varying solder mask patterns on the quality of wafer-level flip chip assemblies particularly with respect to the die misalignment phenomena. Given the importance of underfill filleting with respect to the manufacturability and reliability of flip chip assemblies, a method for defining the shape of the underfill fillet as it flows beyond the perimeter of the chip on the substrate is proposed. The method includes the use of materials on the substrate to define particular patterns around a component site which confine or restrict the underfill as it flows beyond the perimeter of the chip in a flip chip assembly. By creating defined patterns around the substrate site where the die is placed, with materials such as solder mask, it may be possible to control many of the geometric characteristics of the fillet. Designing symmetry into the solder mask pattern surrounding the die is expected to result in symmetric fillets and balanced surface tension forces around the die edges whereby maintaining wafer-level flip chip alignment during reflow. For those chips that may have deviated from their initial position during underfill liquification, the symmetrical solder mask designs could potentially re-align the devices over the substrate pads. The experiment performed seeks to examine the effect of variations solder mask patterns on the alignment and fillet formation of wafer-level flip chip assemblies.

Theory

Forces Acting on a Wafer-Level Flip Chip Die

A number of forces act on a wafer-level flip chip during reflow. Some of these are identical to the forces acting on a no-flow flip chip, as described in earlier work [2]. The forces acting on a wafer-level flip chip assembly, as shown in Figure 3, include:

1) Weight of the chip (W_{chip})

2) Surface tension at the underfill/chip interface ($F_{S.T.}$)

3) Pressure differential of the atmosphere and the underfill bulk, acting over the top and bottom chip surfaces, respectively ($P_a - P_i$).

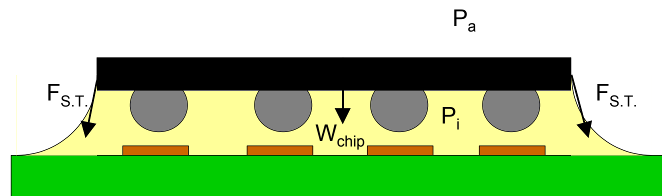

Figure 3. Forces acting on wafer-level flip chip package during liquification and collapse.

The chip weight consists of the weight of the silicon die and attached solder bumps. It is assumed constant throughout the descent of the wafer-level flip chip.

$$W_{chip} = mg \tag{1}$$

where

m = mass of die and solder bumps

g = gravitational acceleration.

The surface tension contribution to the system is due to the meniscus at the edge of the liquid underfill. For a given length of the die as shown in Figure 4, the surface tension force is given by:

$$F_{S.T.x} = L\gamma \sin(\theta_1) \tag{2}$$

$$F_{S.T.y} = L\gamma \cos(\theta_1) \tag{3}$$

where

L = chip length

γ = underfill surface tension

θ_1 = fillet angle at underfill/chip interface.

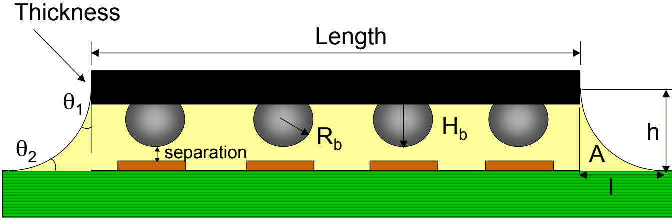

Figure 4. Geometries in wafer-level flip chip system.

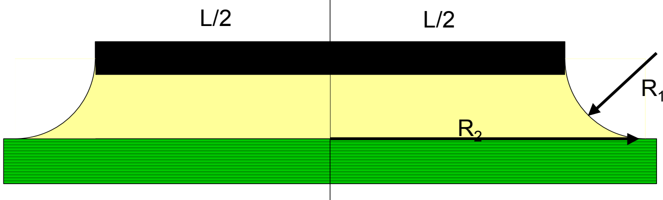

Figure 5. Radii of curvature in flip chip underfill fillets.

The internal pressure of the underfill acting on the chip is determined by the volume of underfill displaced by the chip, the radii of curvature of the liquid/vapor meniscus, and the viscous forces generated in the fluid as the die descends to the substrate. Pressure arises from the buoyancy effect of displaced underfill fluid as the chip descends.

$$F_{buoyancy} = \rho g\left[(h_w)(L^2) + N_b\left(\frac{4}{3}\pi R_b^{\ 3}\right)\right] \tag{4}$$

where

ρ = underfill density

g = gravitational acceleration

h_w = wetted sidewall height of the die

N_b = number of bumps on chip

R_b = bump radius.

Pressure is also generated by the meniscus at the upper corner of the underfill fillet. At the fillet contact point on the chip, there is a concentration of pressure due to the fillet. The pressure acts parallel to the chip sidewall, generating an upward force. The area over which the force acts is the projected area of the chip.

$$P_{meniscus} = \gamma\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{5}$$

$$F_{meniscus} = \gamma\left(\frac{1}{R_1} + \frac{1}{R_2}\right)(L^2) \tag{6}$$

where

R_1 = fillet radius of curvature, major

R_2 = fillet radius of curvature, minor (see Figure 5 for more detail).

In addition, pressure arises from the flow of the viscous underfill. The situation of two disks squeezed together against a fluid, as shown in Figure 6, is analogous to a chip collapsing onto a substrate with liquid underfill separating the two surfaces. For geometric simplicity, the configuration of parallel, circular may be assumed to approximate the system of the typically square die on the substrate. Because the chip is not actually circular, an approximate radius is determined with the following:

$$R = \sqrt{\frac{L^2}{\pi}} \tag{7}$$

where

L = chip length.

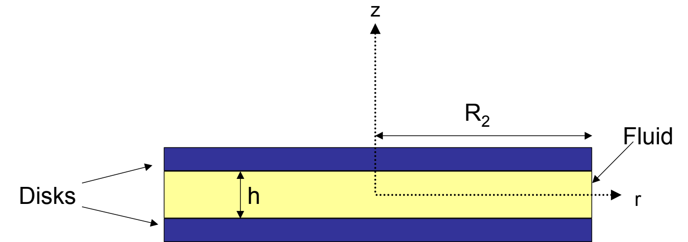

Figure 6. Coordinate system and dimensions for squeeze flow approximation of viscous pressure contribution.

Squeeze flow is a classic fluid mechanics problem with well-established solutions available in numerous publications for both Newtonian and non-Newtonian flow. By definition, squeezing flow is a form of creep flow, characterized by small Reynolds numbers [3]. The flow field established during the collapse of a wafer-level flip chip is a creep flow, due to the low flow velocity, small characteristic length, and relatively high viscosity of the polymer underfill (assumed Newtonian for this order of magnitude analysis). Applying boundary conditions obtained from a force balance on a differential element at the exiting free surface of the flow and integrating over the surface of the upper disk yields the instantaneous force, F, required to attain the instantaneous velocity, dh/dt.

$$F_{viscous} = \frac{3\pi\eta\dot{h}R^4}{2h^3} \tag{8}$$

η = fluid viscosity

h = height of chip above substrate

R = equivalent chip radius.

In summary, the total force contribution by the underfill on the descending flip chip is

$$F_{underfill} = F_{buoyancy} + F_{meniscus} + F_{viscous} \tag{9}$$

where $F_{buoyancy}$ is given by (4), $F_{meniscus}$ is given by (6), and $F_{viscous}$ is given by (8).

Experimental Procedure

Effect of Coating Uniformity on Wafer-Level Flip Chip Assembly Quality

This experiment examines the effect of varying degrees of underfill coating uniformity on flip chip assembly quality. In the experiment, there are four levels of uniformity summarized in Table 1. The levels of uniformity used are based on previously achieved coating qualities that are representative of published application processes. The levels are reported as average surface roughness (R_a). The average coating thickness is 140 μm. There are five replicates for each level of coating roughness. The output effects measured are underfill voids and die mis-alignment.

Table 1. Factors in Process Experiment #1 (The Effect of Coating Uniformity on Flip Chip Assembly Quality)

Factor	Levels (R_a)
Uniformity	10 micron
	20 micron
	25 micron
	30 micron

The test vehicle used for this experiment is a FB-250 daisy chain test die from Flip Chip Technologies. The chip is an 18-mil (~457 micron) pitch, perimeter array, eutectic-solder-bumped test die, measuring 6.3 mm x 6.3 mm. An FR-4 substrate is used in conjunction with the FB-250 test die. The substrate has ten placement sites. In order to maintain die alignment after placement, a small amount of liquid flux is deposited on the substrate site prior to die placement. Because the test underfills exhibit outgassing at temperatures above 150°C, the temperature profile used for all experiments has a low peak temperature of 125°C, which is sufficient to melt the underfill and cause chip collapse.

Effect of Solder Mask Patterns on Wafer-Level Flip Chip Assembly Alignment

This second process experiment examines the effect of varying solder mask patterns on wafer-level flip chip assembly quality. The patterns consists of a central area of solder mask as the intended wetting surface, surrounded by a copper boundary. The copper boundary is mask-defined. The experimental factors are solder mask pattern, underfill viscosity/surface tension, and underfill coating thickness. The levels of the factors are summarized in Table 2. The underfills are denoted as A and B, with B exhibiting better wetting characteristics than underfill A. The coating thicknesses are an average of 50 μm and 110μm above the bump height of the die. The response variable is alignment, which is measured by determining the position of the die with respect to the corners of the photodefined substrate pad site.

A full-factorial experimental matrix with six substrate patterns, two underfill thicknesses, and two underfill types with varying viscosity and surface tension is used. Five replicates of each combination are employed. A total of 120 test die are used in the experiment.

Table 2. Factors in Process Experiment #2 (The Effect of Solder Mask Patterns on Wafer-Level Flip Chip Assembly Alignment)

Factor	Levels
Solder Mask Pattern	6 variants
Underfill (viscosity/ surface tension)	2
Underfill thickness	2

The test vehicle chosen for the process experiments is the Medtronics PA03B-9A test die. The chip is a 16-mil pitch (~406μm), perimeter array, eutectic-solder-bumped test die, measuring 6.3mm x 6.3mm. An FR-4 substrate is used in conjunction with the test die. The substrate is designed to include all of the necessary solder mask patterns for the experiment on a single board. Three symmetric mask shapes are chosen, including a square, a square with rectangular extensions, and a square with arc-shaped extensions, as seen in Figure 7. Two sizes of each mask shape are tested in the experiment, for a total of six solder mask pattern variations.

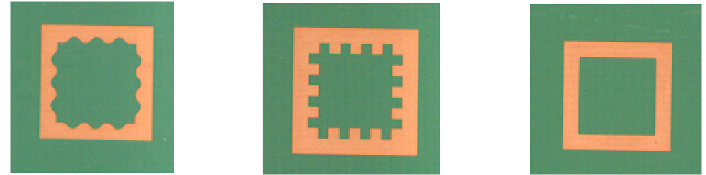

Figure 7. Pattern shapes used in solder mask pattern experiment.

Pattern type 1 and 2 are squares of solder mask with arc-shaped extensions along the four sides. The length and width of the square for type 1 is 7.5mm, and 8.0mm for type 2. The total wettable surface area (solder mask area) for a type 1 site is 64mm^2. The surface area of a type 2 site is 72mm^2. The surrounding copper border is mask-defined.

Type 3 and 4 patterns are squares with rectangular extensions along the four sides. Type 3 is 7.0mm x 7.0mm, with a surface area of 64mm^2. Type 4 is 7.5mm x 7.5mm, with a surface area of 72mm^2. The surrounding copper border is mask-defined.

Patterns 5 and 6 are squares with surrounding copper borders. Type 5 is 7.5mm x 7.5mm with a wettable area of 56mm^2, and type 6 is 8mm x 8mm with a wettable area of 64mm^2.

Results

The Effect of Coating Uniformity on Wafer-Level Flip Chip Assembly Quality

Figure 8 depicts a C-SAM image showing the effects of level 1 coating uniformity on a typical wafer-level underfill flip chip assembly. The large circular artifact in the center of the image is the flux that is dispensed on the site. Because the temperature profile has a low peak temperature, the flux does not reach its activation temperature and remains distinctly separate from the underfill. All of the samples exhibit a

distinct separation of the underfill and added flux upon C-SAM analysis. The distorted areas on the left and top edges of the die in Figure 8 are areas of underfill contamination on the top of the assembly (back side of the die).

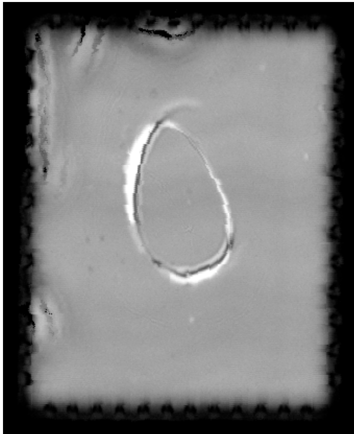

Figure 8. C-SAM image of level 1 coating uniformity wafer-level assembly.

In contrast, the effect of a typical level 4 coating uniformity on a typical wafer-level underfill flip chip assembly is shown in Figure 9 indicating more voiding. The flux can be seen in three distinct droplets. Possibly due to the severity of voiding, the original flux droplet is separated into three pieces during underfill liquification. It can be seen that much of the voided region is near one edge of the die, which is consistent with previous experience in wafer-level assembly. The entrapped gas tends to collect together and migrate to an edge of the die where it can escape to the atmosphere. The voiding data collected from the experiment is presented in Table 3.

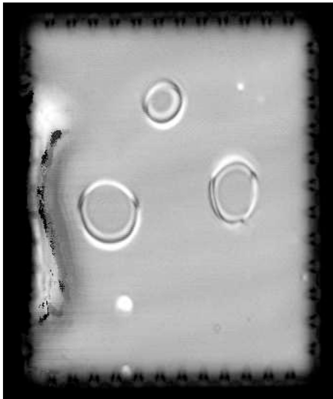

Figure 9. C-SAM image of level 4 coating uniformity wafer-level assembly.

Table 3. Voiding data for coating uniformity experiment.

Roughness (level)	Voiding (#)	Roughness (level)	Voiding (#)
1	0	3	5
1	1	3	4
1	2	3	5
1	1	3	5
1	1	3	3
2	2	4	5
2	3	4	7
2	1	4	8
2	5	4	4
2	3	4	6

To compare the effects of coating uniformity on voids, a main effects plot is generated and shown in Figure 10. The ANOVA (analysis of variance) model used a Minitab version 12.1 statistical software analysis is the General Linear Model. As the plot shows, coating uniformity has a clear effect on the level of voids observed in the sample. The variance of the data is plotted in Figure 11, with the bars representing standard error.

Main Effects Plot - Data Means for Voids

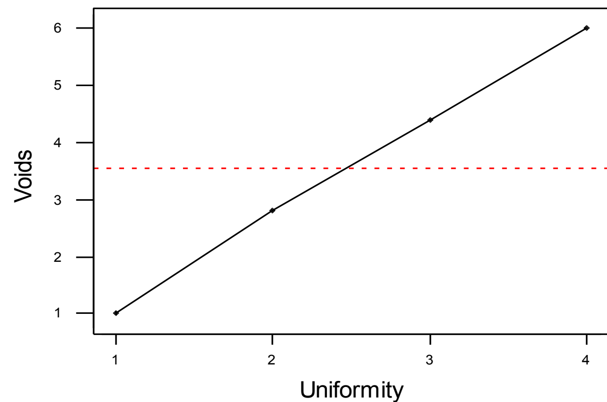

Figure 10. The effect of coating uniformity on voids in wafer-level flip chip assemblies.

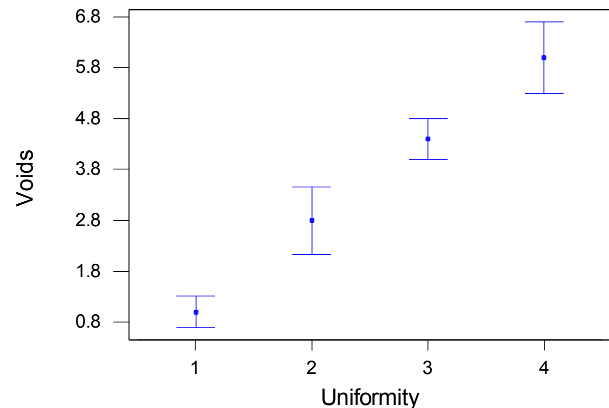

Figure 11. Variation in data for the effect of coating uniformity on voids in wafer-level flip chip assemblies.

After performing ANOVA for the effect of coating uniformity on voids, a p-value of less than 0.001 is obtained. Thus, the null hypothesis, that the amount of voiding for each treatment is the same, can be rejected. It is concluded that coating uniformity has an effect on the voiding in the experimental assemblies, with better coating uniformity (i.e., less average roughness of the coated surface) resulting in a lower percentage of underfill voids in the sample wafer-level flip chip assemblies.

To determine the alignment of the die after assembly and underfill melting, the test vehicle assemblies are inspected with a FeinFocus x-ray inspection system (Model FXS 100/25). The alignment measurements are presented in Table 4. Based on the results of the ANOVA, there is no correlation between misalignment and coating uniformity level. The random nature of the coating roughness is demonstrated in the random nature of the measured misalignment for each sample. There is no general trend toward misalignment in any particular direction. The mechanism for misalignment due to coating roughness is primarily void growth, bubble coalescence, and void movement. The random nature of these void-related phenomena suggests that any observed die misalignment should be random as well.

Table 4. Misalignment data for coating uniformity experiment

Uniformity (level)	X Offset (mils)	Y Offset (mils)
1	1	-2.5
1	3	-4
1	3	3
1	3.5	0.5
1	-2.5	2
2	9	-7
2	2	-2.5
2	-6	9
2	-3.5	0
2	1	-4.5
3	1.5	4
3	2	1
3	2.5	-3
3	2	-1
3	-0.5	0.5
4	5	-3
4	-4	-4
4	0	0.5
4	0	1.5
4	5	3.5

The Effect of Solder Mask Patterns on Wafer-Level Flip Chip Assembly Alignment

Having previously seen misalignment in wafer-level flip chip assemblies during reflow, an experiment is conducted to determine if geometric patterns in the substrate can reduce or eliminate die movement.

After performing the experiments, it is observed that none of the samples wet beyond their patterned solder mask borders indicating that the defined patterns were effective in serving as a fillet dam on the substrate. However, a majority of the samples do not exhibit full wetting up to the edge of the solder mask border on all four sides. Of the 120 total samples, 45 wet out making symmetrical contact with portions of the border on all four sides and having constrained fillets. None of the patterns are completely filled with underfill, as the surface tension of the underfill does not permit highly irregular fillet shapes. The remaining 75 samples do not wet to the edge of the borders. The primary reasons for this are insufficient underfill capillarity and/or insufficient coating thickness to fully wet a given patterned area.

Of the four underfill/thickness combinations, the samples coated with 110μm of underfill B achieve the most consistent wetting, as seen in Table 5, with 29 of 30 such samples exhibiting full wetting of the patterned site out to the surrounding border. In contrast, both of the coating combinations involving underfill A are relatively ineffective at promoting full substrate site wetting.

Table 5. Number of fully wetted samples per underfill/coating thickness combination.

Underfill	Coating thickness (μm)	Fully wetted samples	Total samples	Percentage of fully wetted samples
A	50	0	30	0.0
A	110	3	30	10.0
B	50	13	30	43.3
B	110	29	30	96.7

Regarding the pattern type, pattern 3 results in the most samples that wet the substrate site to the border on all four sides (see Table 6). Pattern type 6 has the fewest samples that fully wet the substrate site, because of the large amount of wettable pattern area within the square ($64mm^2$). Although pattern types 2 and 4 technically have more solder mask patterned area ($72mm^2$) than pattern type 6 ($64mm^2$), they essentially have less "wettable" pattern area since the underfill cannot fully wet around the irregularities in patterns 2 and 4 due to surface tension and minimum area requirements. This effect can be seen in Figure 12.

Table 6. Number of fully wetted samples per underfill/coating thickness combination.

Pattern type	Fully wetted samples	Total samples	Percentage of fully wetted samples
1	5	20	25.0
2	5	20	25.0
3	13	20	65.0
4	9	20	45.0
5	9	20	45.0
6	4	20	20.0

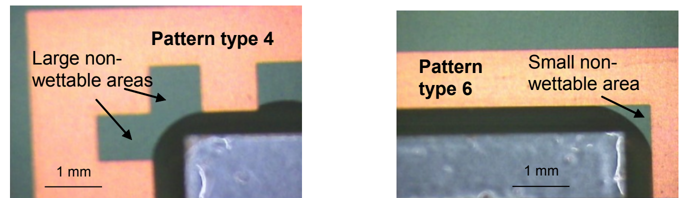

Figure 12. Comparison of wetting for pattern type 4 and pattern type 6.

Die alignment is determined by measuring the distance from the corners of the square die to the corners of the symmetric patterns, for each of the 120 samples. The X- and

Y-offset values can be measured directly, and the theta-offset (rotation) can be calculated indirectly. X- and Y-offset values are reported as misalignment distance of the die from the center of the site in microns, with positive values indicating misalignment to the right or above the pattern's center, respectively, and negative values indicating misalignment to the left or below center, respectively. Positive theta values indicate clockwise rotation. See Figure 13 for a representation of the coordinate system.

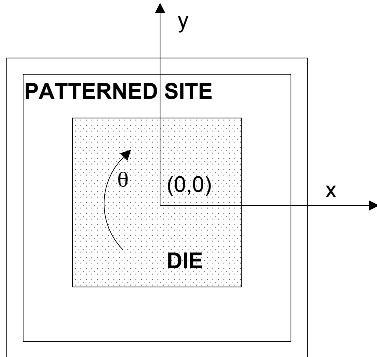

Figure 13. Coordinate system for misalignment measurements in process experiment #2.

A summary of the misalignment data is seen in Table 7. The relatively small mean X-offset is as expected. However, the much larger mean Y-offset suggests that an outside factor may affect these results. After further investigation, it is determined that the substrate experiences warpage in such a way as to promote Y-offset.

Table 7. Summary of misalignment data for experimental population.

	Mean	Standard Deviation
X-offset (μm)	3.0	6.1
Y-offset (μm)	-44.5	-39.7
Theta-offset (°)	0.269	0.220

Figure 14 presents a main effects plot for the effect of full substrate wetting on Y-offset. The main effects plot seems to show a strong influence of full substrate site wetting of die on the amount of Y-offset. Full wetting samples have an average Y-offset of –16.8μm, while the incomplete wetting samples have an average y-offset of –61.6μm. It is likely that full substrate site wetting is important in determining the misalignment. The fully wetted samples better resist the potential for misalignment that is posed by the warped substrate.

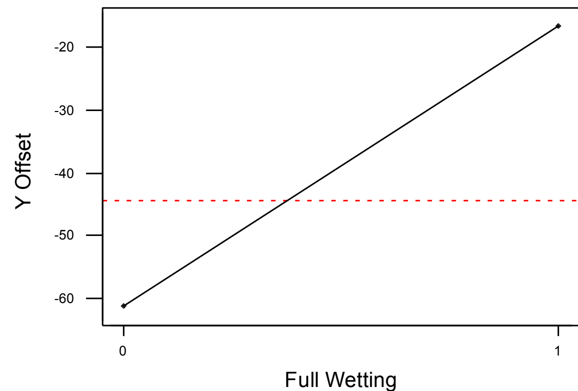

Figure 14. The effect of full wetting on Y-offset.

Discussion

Having designed an experiment to determine the effect of underfill coating uniformity on wafer-level flip chip assembly quality, conclusions about the significance of coating uniformity can be made. The coating uniformity is determined to have an effect on the voids in the melted assembly, with increasing roughness resulting in increasing voiding of wafer-level flip chip assemblies. This result is expected, since the increase in roughness represents an increase in the number of coating asperities that can potentially lead to entrapped pockets of air upon underfill liquification. Conversely, coating uniformity is found to have no effect on the alignment of the die. It is reasonable not to see any general trends in misalignment due to voiding, as void coalescence and movement are random in nature and do not influence die shift in any particular direction. In general, underfill coating roughness should be minimized to prevent underfill voids in wafer-level flip chip assemblies.

To ensure void-free assemblies, an average underfill coating roughness of no more than 10μm is suggested as a process window. With an average roughness value of 10μm, the level 1 uniformity samples display minimal to no voiding during package liquification. These samples also are affected by the liquid flux and entrapped air bubbles prior to underfill coating, so they can reasonably be expected to be free of voids if those influences can be eliminated.

In determining the average coating roughness, the roughness of the substrate should be considered as well, for it is the combined effect of the asperities in the joining surfaces that governs the magnitude of underfill voiding. The substrate sites in this experiment are measured to have an average roughness of 8μm, but substantial deviations from this roughness will narrow or widen the window of tolerable underfill coating roughness. For example, a substrate with a surface roughness less than 8μm would be expected to increase the allowable average roughness of the underfill coating as determined in this experiment. Conversely, much rougher substrates are expected to decrease the average coating roughness that can be recommended for void-free package wetting and collapse.

Previous work has shown that underfill voids often coalesce during underfill liquification in wafer-level flip chip

assemblies. By combining into a relatively large void, the entrapped air threatens alignment as the temperature increases. Because the bubble can be anticipated to increase in volume as the temperature increases, a large void that expands to a diameter of greater than the bump height can have enough internal pressure to lift one edge of the die away from the substrate pads. In addition, the underfill viscosity decreases with increasing temperature, thus reducing viscous resistance to bubble translation through the underfill bulk. At temperatures approaching and exceeding the melting temperature of solder, the size and movement of voids would probably be more severe than at the lower temperature range that is associated with underfill liquification and chip collapse. The voiding may not display general trends of die misalignment or die lifting in a particular direction with respect to the substrate site. On the contrary, the defects that do occur (i.e., die floating, lifting, misalignment) will likely appear to be random in nature. Regardless, the presence of voids in the underfill coating during wafer-level flip chip assembly should be avoided as they are detrimental to successful interconnect formation.

Furthermore, FR-4 substrates can absorb moisture during storage, which can volatilize during reflow of the assembly and introduce voids in the underfill. To eliminate the possibility of evaporation of absorbed water during reflow, it is recommended to bake the substrates at 125°C for at least two hours.

If the underfill coating uniformity and substrate bake out requirements are met, wafer-level flip chip assembly with minimal or no underfill voiding appears to be readily achievable for manufacturers. Assemblers have control over many parameters that affect underfill voiding in wafer-level flip chip assemblies, but assembly problems associated with underfill chemistry, such as flux-related outgassing, can only be addressed by material suppliers

A method to constrain fillet wetting length for fillet symmetry and self-alignment is proposed, with the concept implemented using conventional solder mask processing techniques. The resulting experimental analyses demonstrates the importance of underfill capillarity in governing fillet wetting, identifies the combination of underfill properties and coating thickness as an important interaction in alignment, and suggests symmetrically constrained fillets may improve wafer-level flip chip alignment. The results also show that full substrate site wetting tends to reduce the misalignment experienced by a wafer-level flip chip during underfill wetting.

The effectiveness of solder mask patterns in constraining fillet wetting is dependent on several factors, including die geometry, coating thickness, wetted fillet length, wettable pattern area, and underfill contact angle on solder mask and the barrier material (e.g., copper). The acceptable range of these factors is determined in the following analysis.

The successful combination of the aforementioned parameters will result in an assembly that fully wets the substrate site so that fillet length is constrained, while maintaining concave fillets so that die floating is not likely to occur. In order to generate a process window that results in an acceptable combination of the factors, the minimum requirements of wetting to the barrier are discussed.

The minimum condition of underfill wetting to the surrounding border of the substrate site is analogous to achieving a fillet length equal to the allowable fillet length as defined by the pattern. Figure 15 shows the allowable fillet length, which is defined by geometry as

$$allowable\ fillet\ length = \frac{\left(length_{site} - length_{die}\right)}{2} \tag{10}$$

Using the circular fillet approximation, the coating thickness required to generate a fillet length equal to the allowable fillet length can be found for any die/underfill combination. The upper limit of the process window is determined by considering the combination of factors that results in the underfill wetting beyond the intended area and onto the surrounding border. As the underfill wets and the fillet length reaches the allowable length defined by the substrate pattern, fillet length becomes constrained. With fillet height determined by the die geometry and fillet area determined by the coating thickness, the only variables are θ_1 and θ_2, which are the underfill/die and underfill/substrate contact angles respectively. As more fillet area is added (i.e., coating thickness is increased), the contact angles must increase, since the fillet height and length are constrained. The actual limit on the process is the value achieved by the contact angles. If θ_1 increases to the point where the fillet profile is no longer concave, then die floating becomes a concern. Thus, only ranges of coating thicknesses that result in concave fillets are considered in this analysis.

In addition, θ_2 has an upper limit. For the equilibrium case considered here, θ_2 maintains some specific static contact angle on the wettable surface, which is a function of the underfill and the substrate and can be measured directly. However, an increase in coating thickness generates an increase in θ_2, as the fillet length is constrained by the border and cannot advance. θ_2 can increase up to the value of static contact angle that it displays for wetting on the barrier material, at which point the chemical motivation for constraint is overwhelmed by minimum surface energy considerations. As long as θ_2 remains below its measured value of static contact angle for the barrier material, the underfill meniscus will be constrained and the profile and contact angles will adjust to accommodate increasing fillet area. Thus, the upper limit on θ_2 is equal to the static contact angle for the underfill on the barrier surface.

To determine process windows for the implementation of the solder mask patterns, the previously discussed upper and lower limits on coating thickness are applied. In Figure 16, the variation in underfill/substrate contact angle (θ_2) is plotted over a range of coating thicknesses. Each separate curve corresponds to a particular allowable fillet length, as defined by the pattern size. The lower black bar in Figure 16 is the lower limit on the process, as defined by the contact angle that the underfill makes with the wettable surface. This static contact angle is dependent on the properties of the underfill and the wettable surface and is determined by experimental measurement. The upper black bar represents the upper limit on the process. The upper limit is defined by the static contact angle that the underfill displays when wetting on the barrier surface. Again, the static contact angle is a function of

the properties of the underfill and the barrier surface and is determined experimentally. The values of static contact angle are unique to each underfill/surface combination and can be directly applied as the upper and lower limits for the process window. In the following examples, the upper and lower limits are taken to be 30° and 15°, which corresponds to underfill B.

Regions below the window defined in Figure 16 correspond to incomplete substrate wetting. Regions above the process window represent underfill wetting beyond the intended wetting area. The curves are plotted over a range of reasonable coating thicknesses such that concave fillets are predicted, in order to avoid potential die floating. Figure 16, 17, and 18 depict design windows for FB-250, PB8-2, and FA10-4 die, respectively (see Table 8 for die geometries).

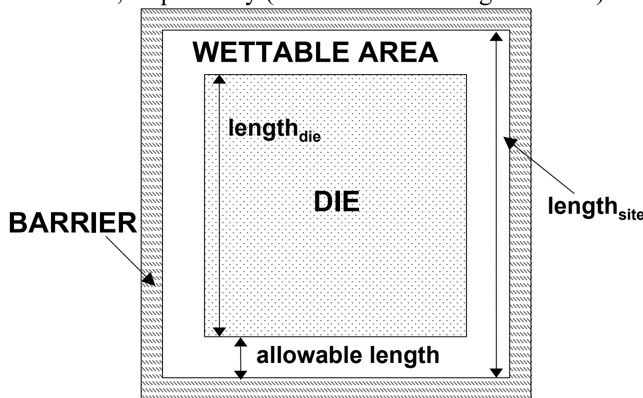

Figure 15. Wetting constraint imposed by solder mask pattern.

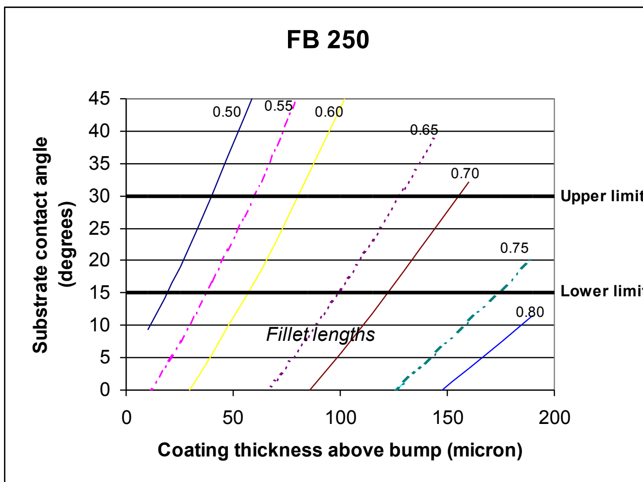

Figure 16. Solder mask pattern design window for FB-250 die.

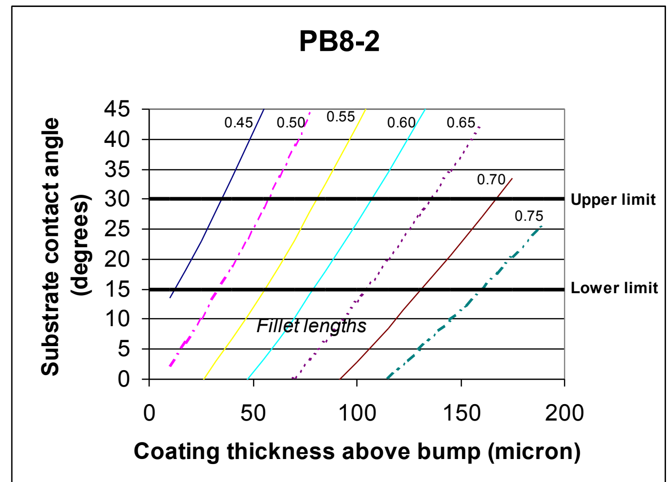

Figure 17. Solder mask pattern design window for PB8-2 die.

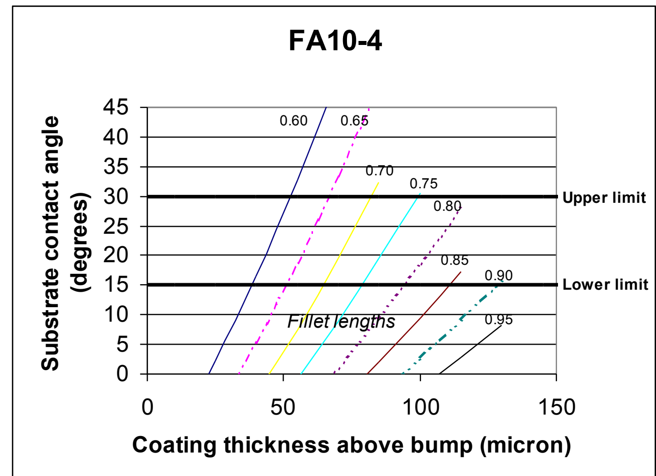

Figure 18. Solder mask pattern design window for FA10-4 die.

Conclusion

By evaluating the effect of coating uniformity on wafer-level flip chip assembly quality, recommendations can be made for the average coating roughness required to attain void-free assemblies. A discussion of the negative effect of voids on wafer-level assemblies underscores the need to minimize or eliminate underfill voids from wafer-level flip chip assemblies.

Based on the results of the underfill coating uniformity study, decreasing average roughness of the coating corresponds to fewer voids in the wetted wafer-level flip chip. For the lowest level of average roughness (10 μm), most of the experimental samples are free of voids after underfill wetting. It is recommended that a production coating process achieve at least this level of coating uniformity to avoid the problem of underfill voiding.

Also, the evaluation of a method to constrain fillet wetting and reduce die misalignment by the use of solder mask patterns is made. This evaluation suggests the trend of reduced misalignment for die with constrained fillet lengths. In order to have constrained wetted length, the substrate site must be fully wetted by underfill. Design guidelines for generating solder mask patterns of appropriate size are

introduced, with the condition of constrained fillet length as the criterion for success. The upper and lower limits on the design window represent wetting beyond the border of the intended wetting area and incomplete wetting of the intended area, respectively. In determining the design windows, die geometry, underfill/substrate contact angles, coating thickness, and pattern size are included as factors. Design windows for three test die are generated, but windows can be created for any test die or underfill, provided that the relevant geometric features or wetting characteristics are known.

References

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Table 8. Geometric properties for selected test die.

Test die	Array type	Die thickness (μm)	Length (mm)	Width (mm)	Bump height (μm)	Bump radius (μm)	Number of bumps
Medtronics	Perimeter	630	6.3	6.3	110	70	56
FB250	Perimeter	560	6.3	6.3	140	95	48
FB500	Perimeter	560	12.7	12.7	140	95	96
PB8-2	Perimeter	560	5.08	5.08	98	60	88
FA10-2	Area	560	5.08	5.08	110	67.5	317
FA10-4	Area	560	10.16	10.16	110	67.5	1268